

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

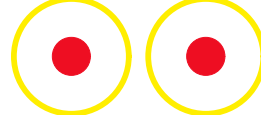
U_PWR2
PWR2.SchDoc

Serial
Serialnumber 6,3 x 6.3mm

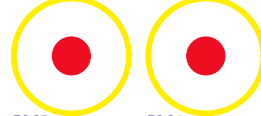
FIDU-DOT - small FIDU-DOT - small



PM1 PM2
FIDU-DOT - small FIDU-DOT - small

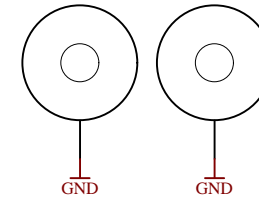


PM3 PM4
FIDU-DOT - small FIDU-DOT - small

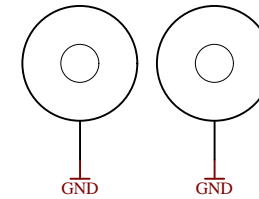


PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm




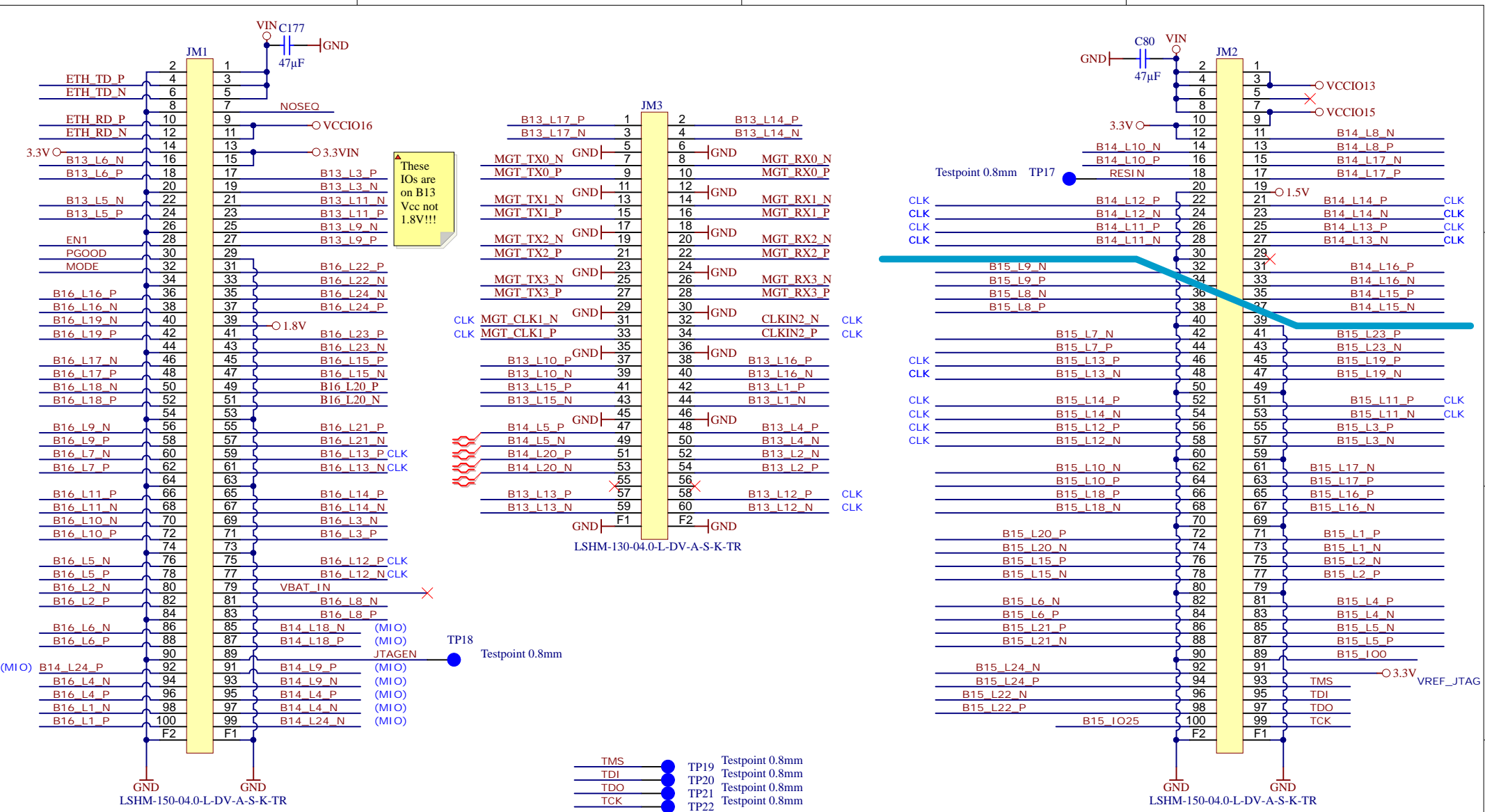
Mount.Hole 3.2mm Mount.Hole 3.2mm



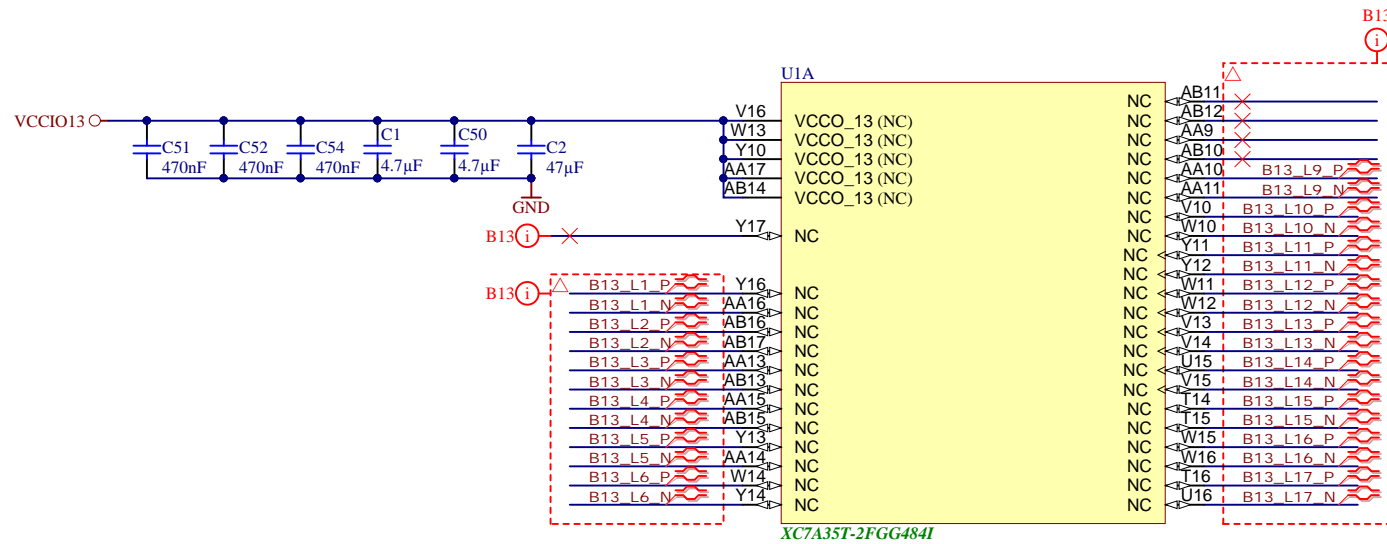
Top of Board



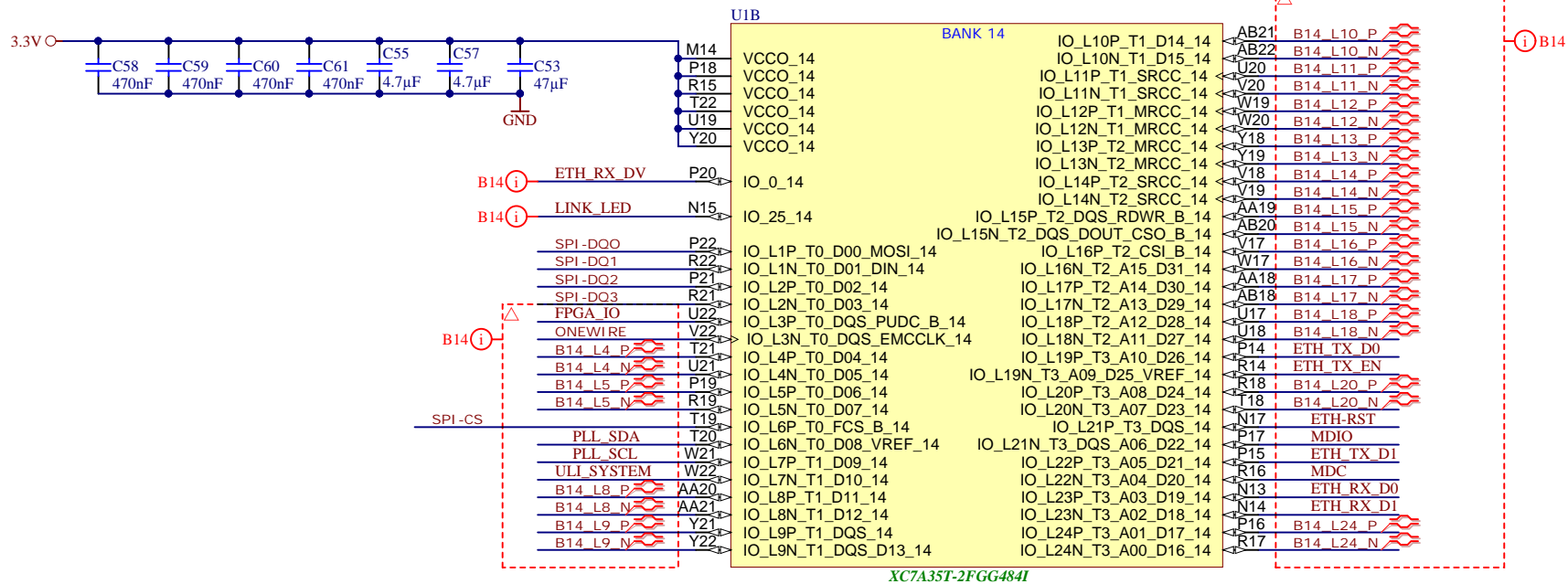
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		A4	Number: TE0712 35-2I
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Filename: TE0712.SchDoc		Page 1 of 16	



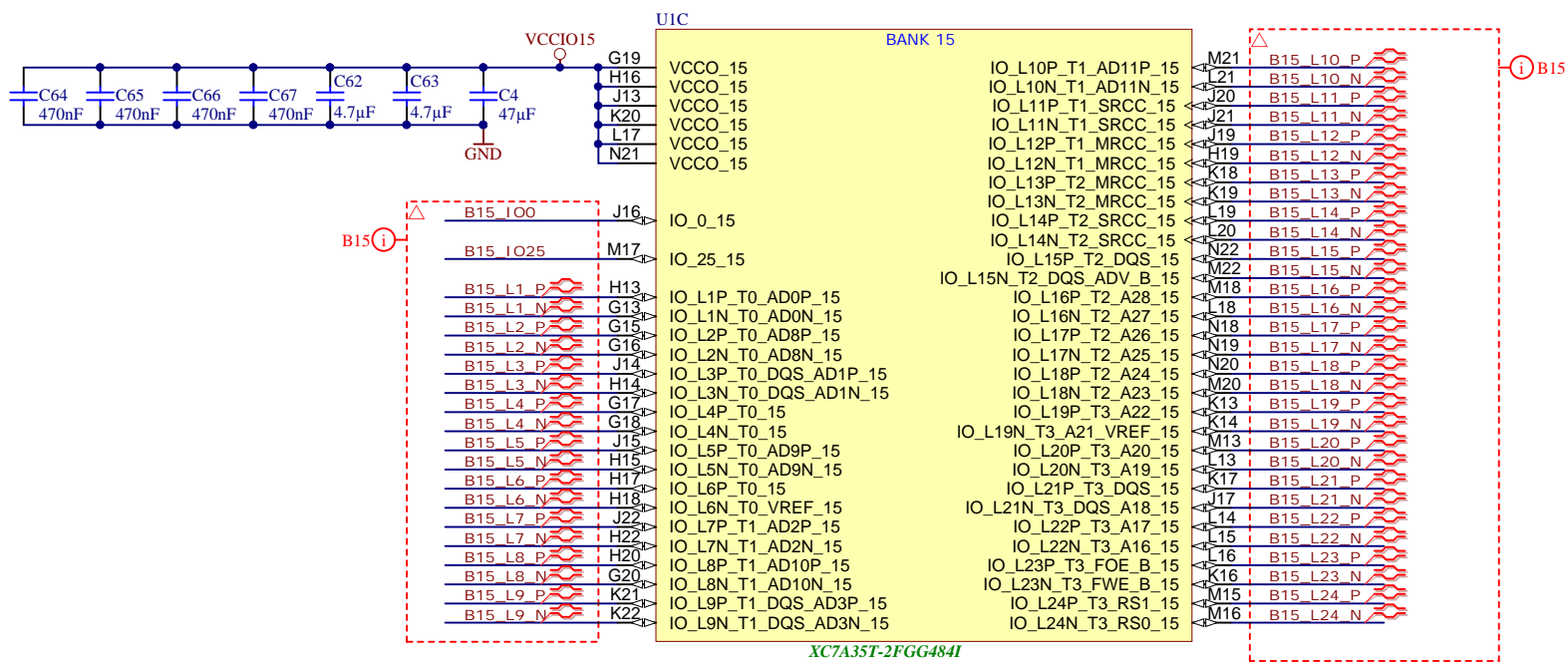
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A4	Number: TE0712 35-21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page2 of 16
Filename: B2B-Connectors.SchDoc		



	Title: B13	
	A4	Number: TE0712 35-2I
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH
	Rev. 02	Page 3 of 16
Filename: B13.SchDoc		



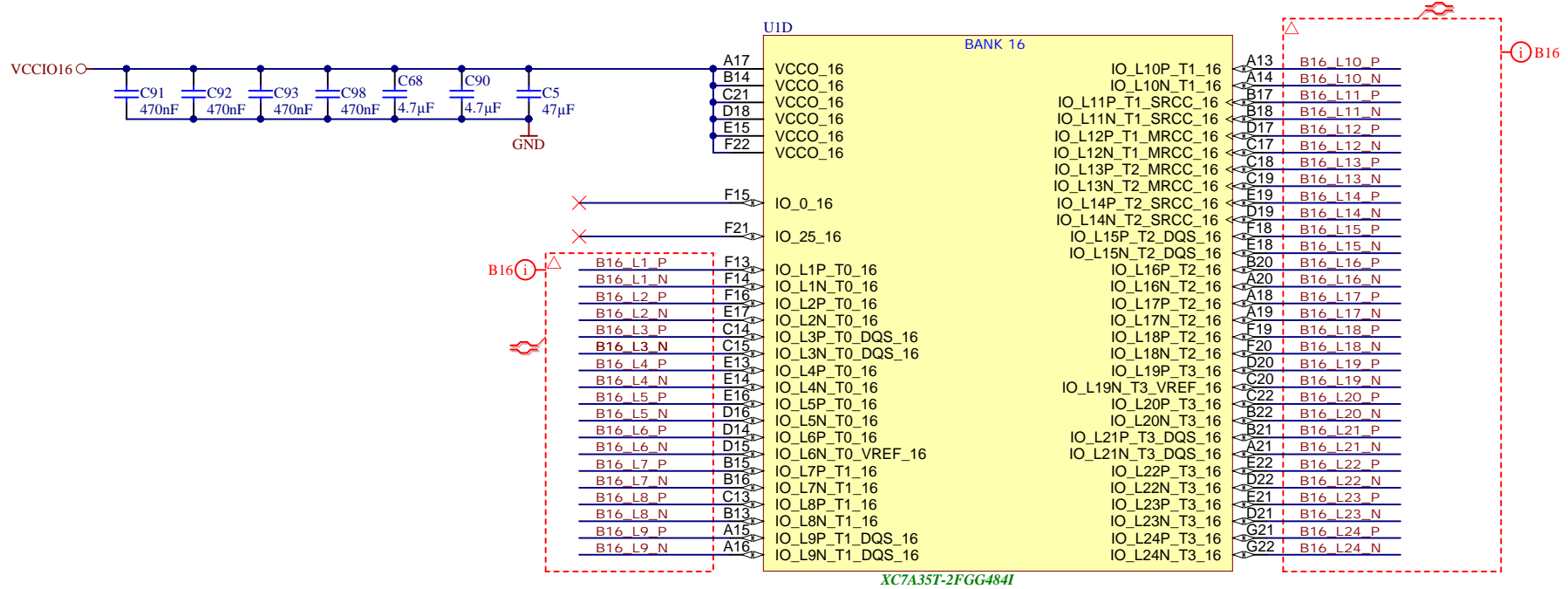
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
Page 4 of 16		Filename: B14.SchDoc



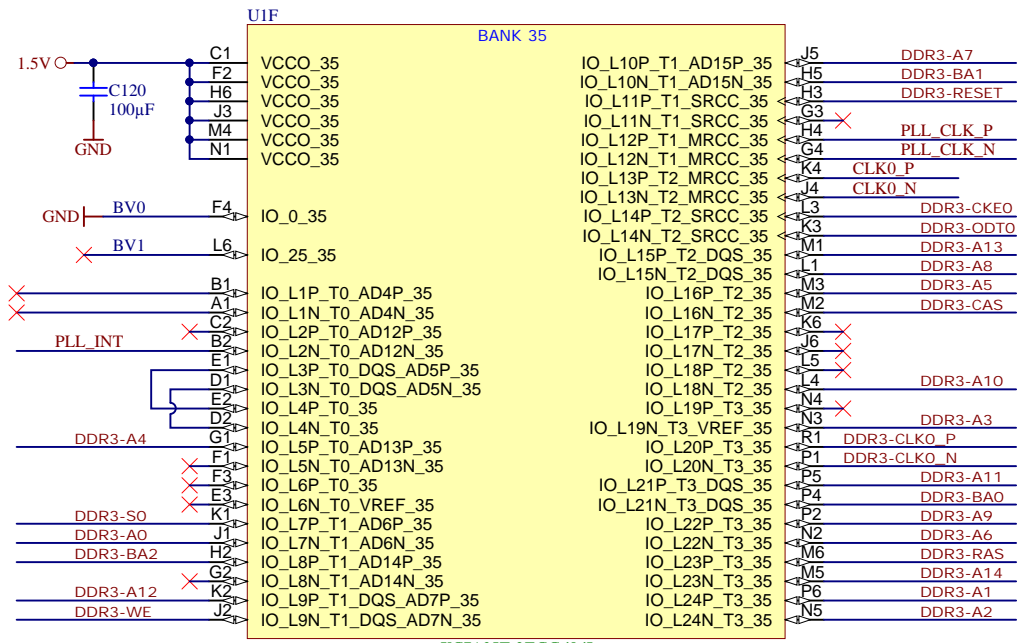
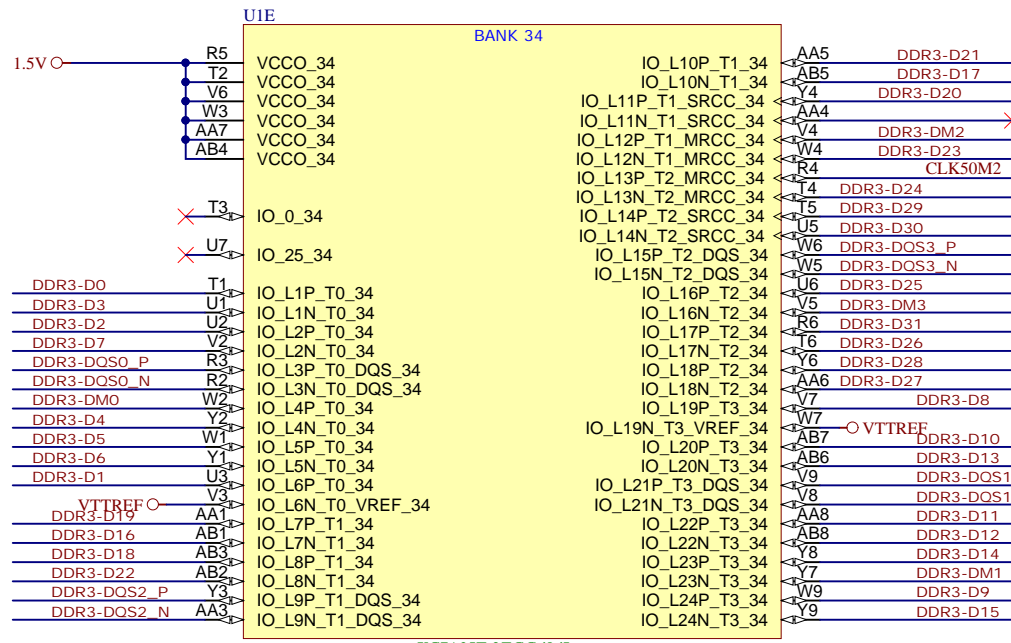
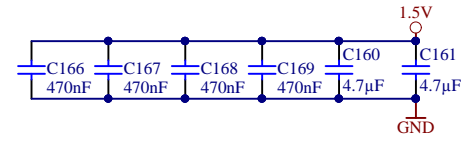
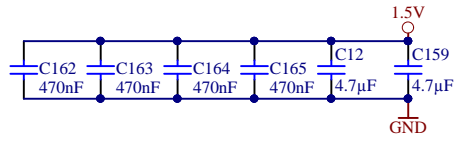
XC7A35T-2FGG484I



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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 5 of 16
Filename: B15.SchDoc		

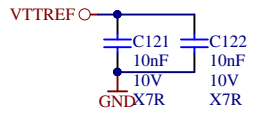
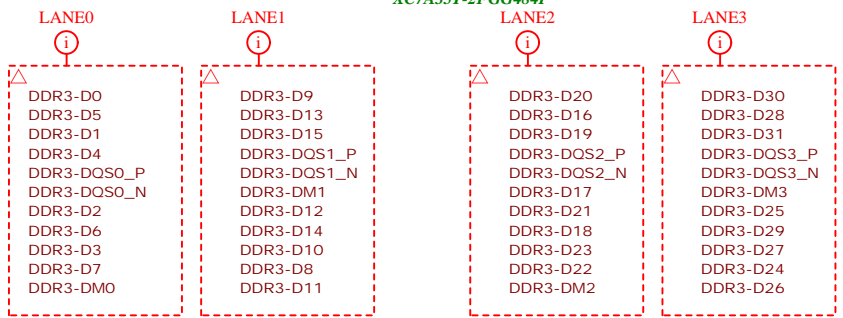


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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 6 of 16
Filename: B16.SchDoc		

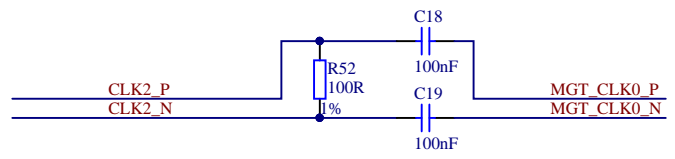
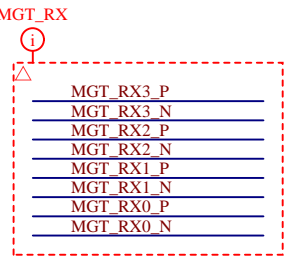
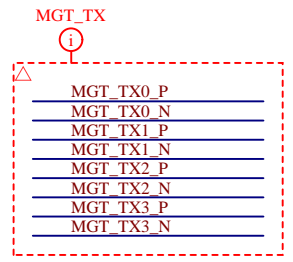
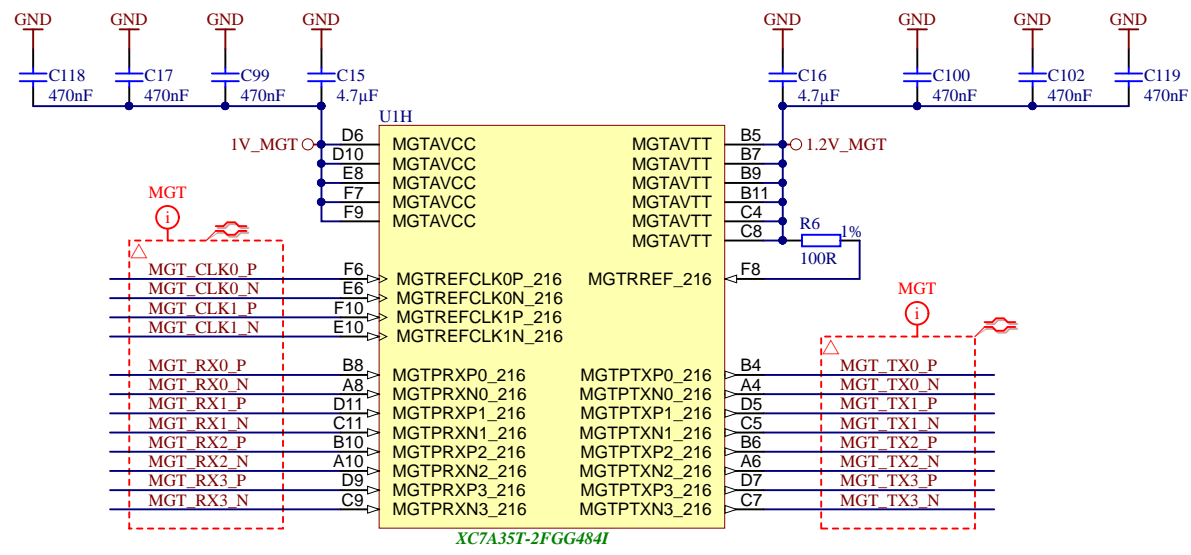


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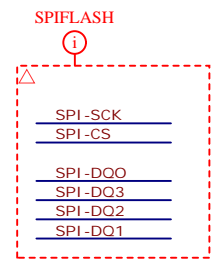
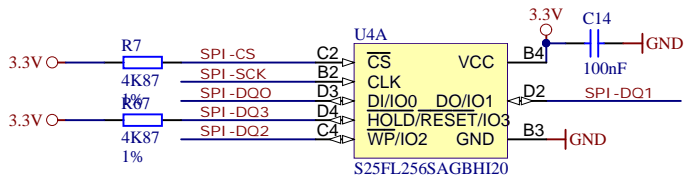
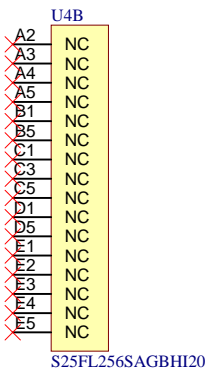
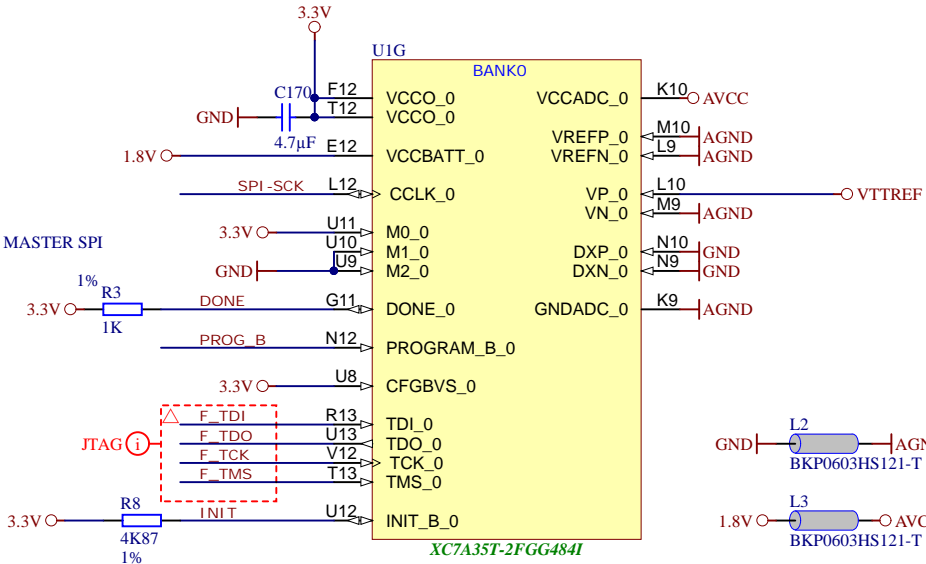
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 7 of 16
Filename: B34.SchDoc		



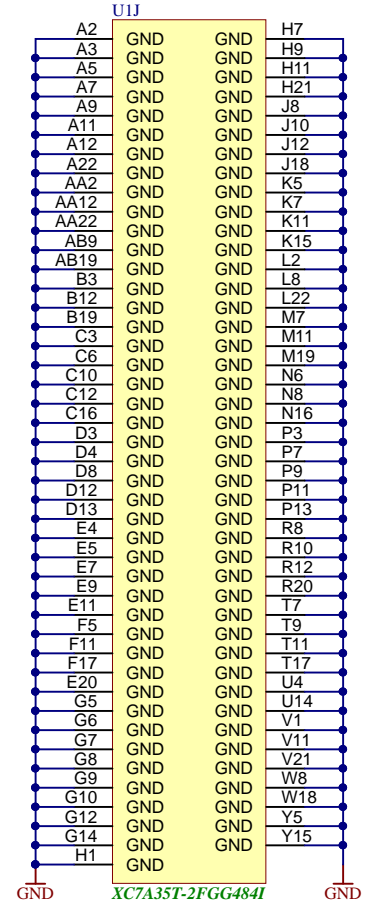
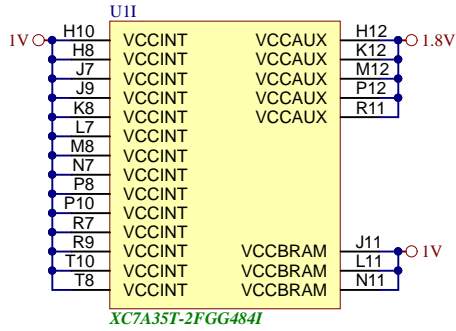
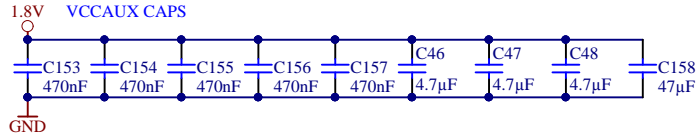
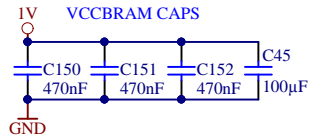
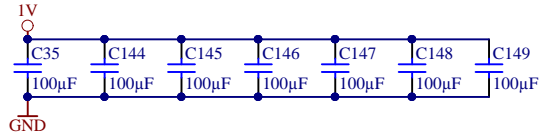
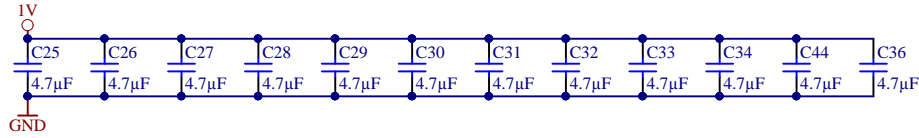
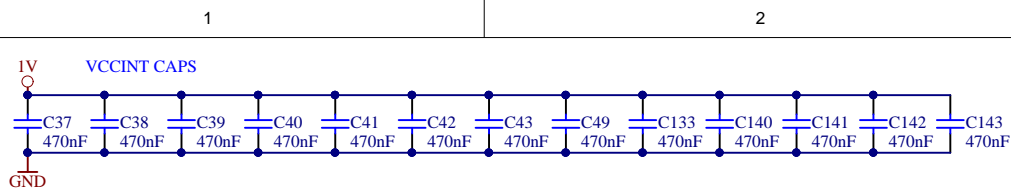
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A4	Number: TE0712 35-21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 8 of 16
Filename: FPGA-MGT.SchDoc		



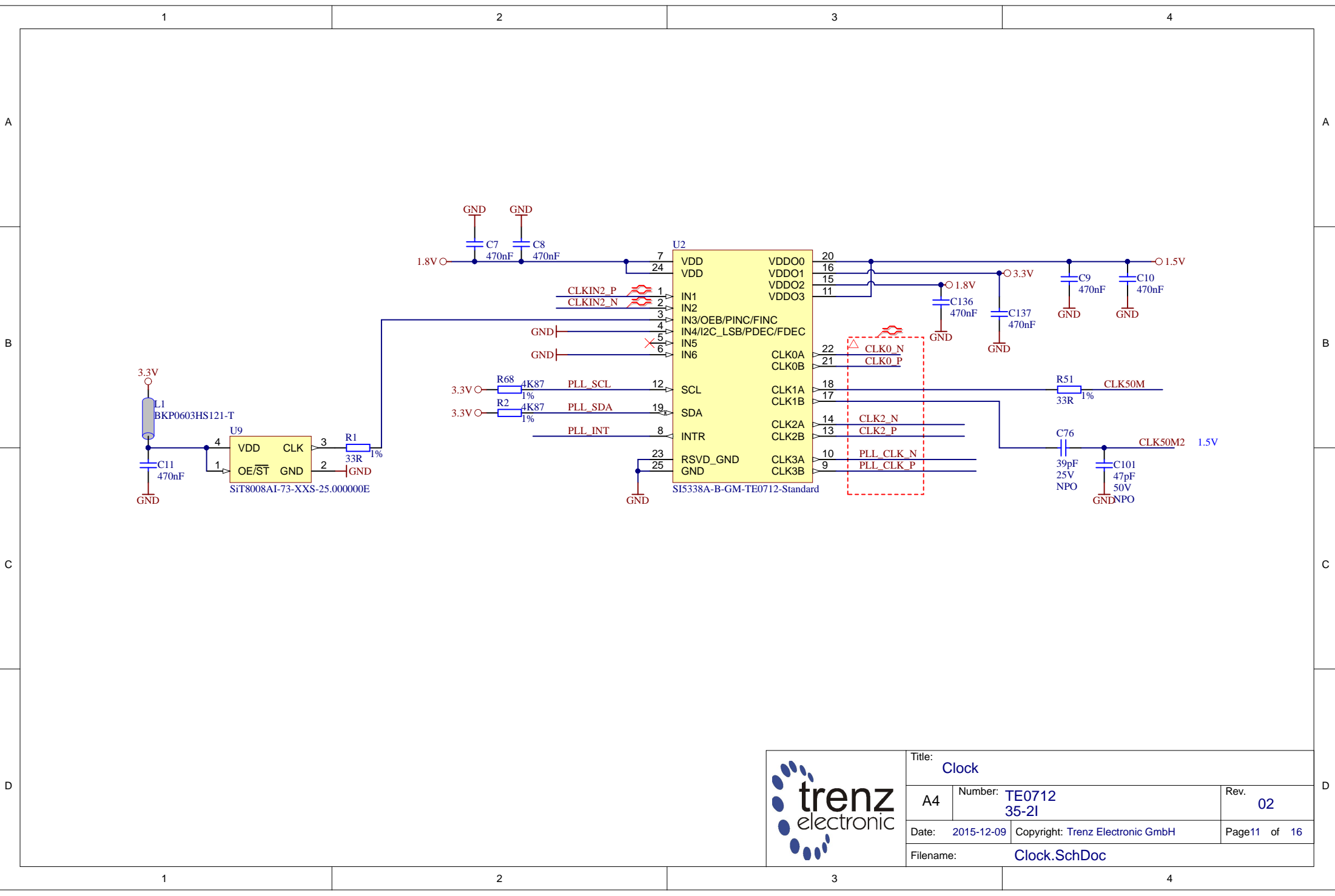
BOOTMODE = MASTER SPI




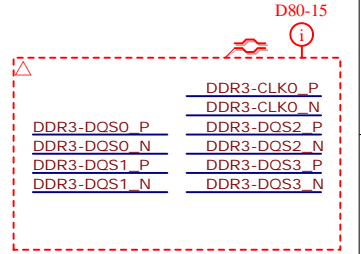
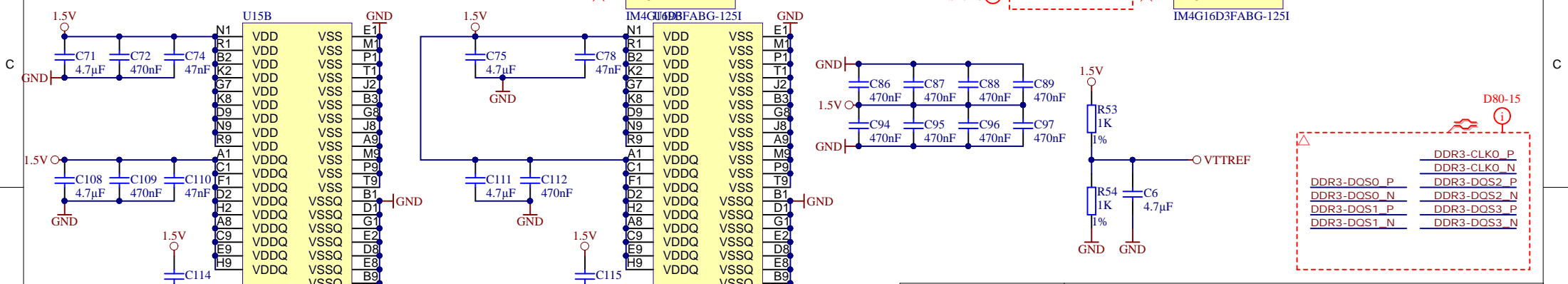
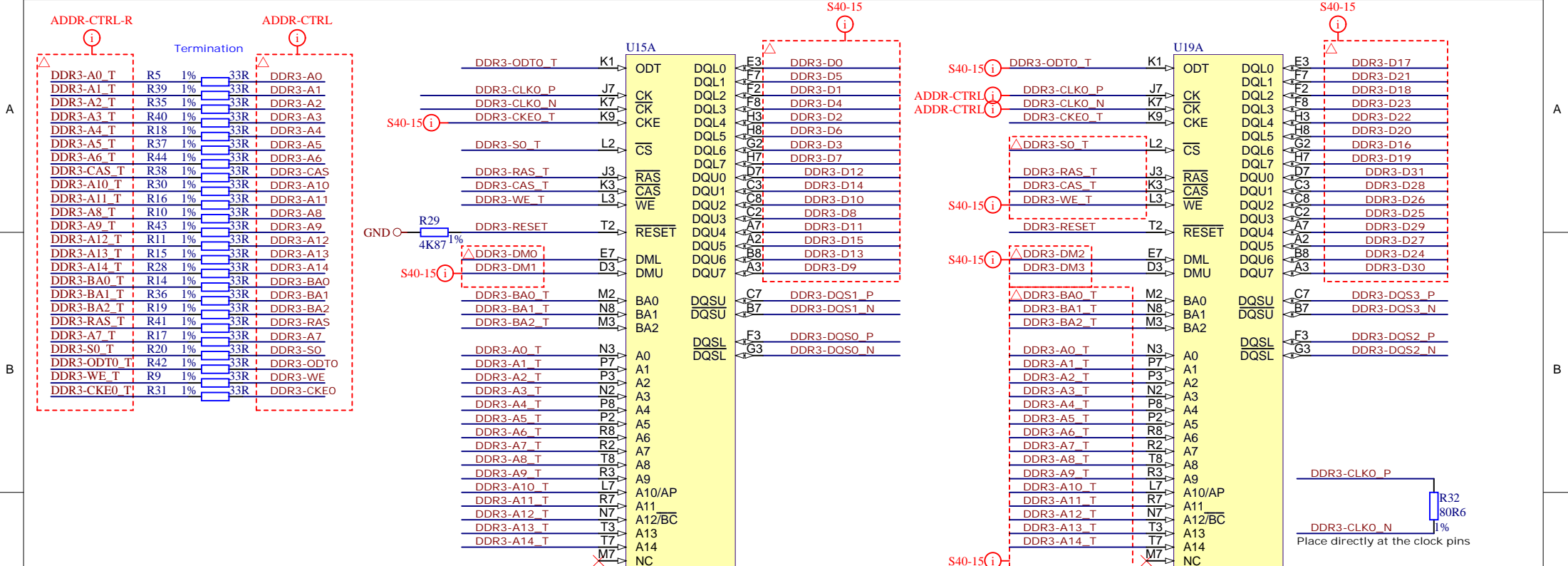
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A4	Number: TE0712 35-21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page9 of 16
Filename: FPGA-CFG.SchDoc		



Title: PWR		
A4	Number: TE0712 35-2I	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page10 of 16
Filename: FPGA-PWR.SchDoc		



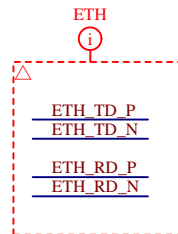
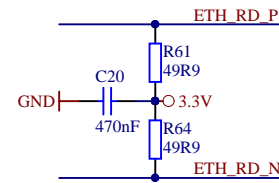
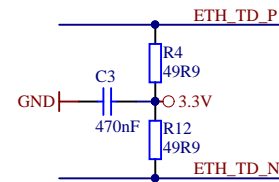
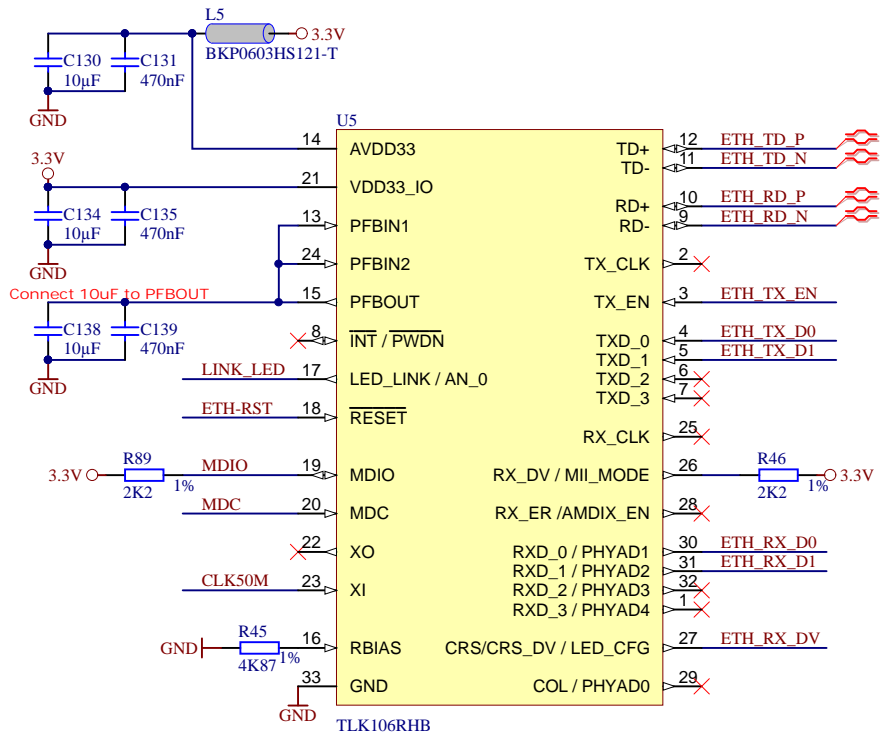
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			A4	Number: TE0712 35-2I
Date: 2015-12-09		Copyright: Trenz Electronic GmbH		Page 11 of 16
Filename: Clock.SchDoc				




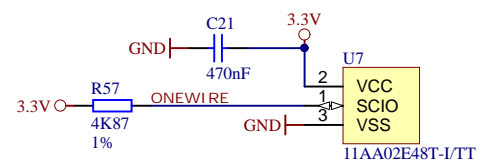
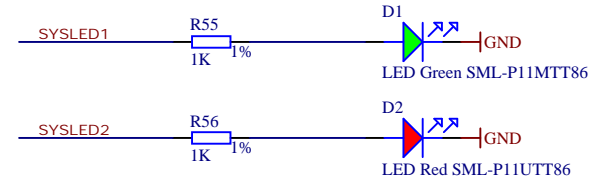
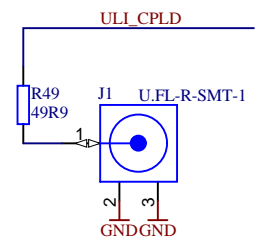
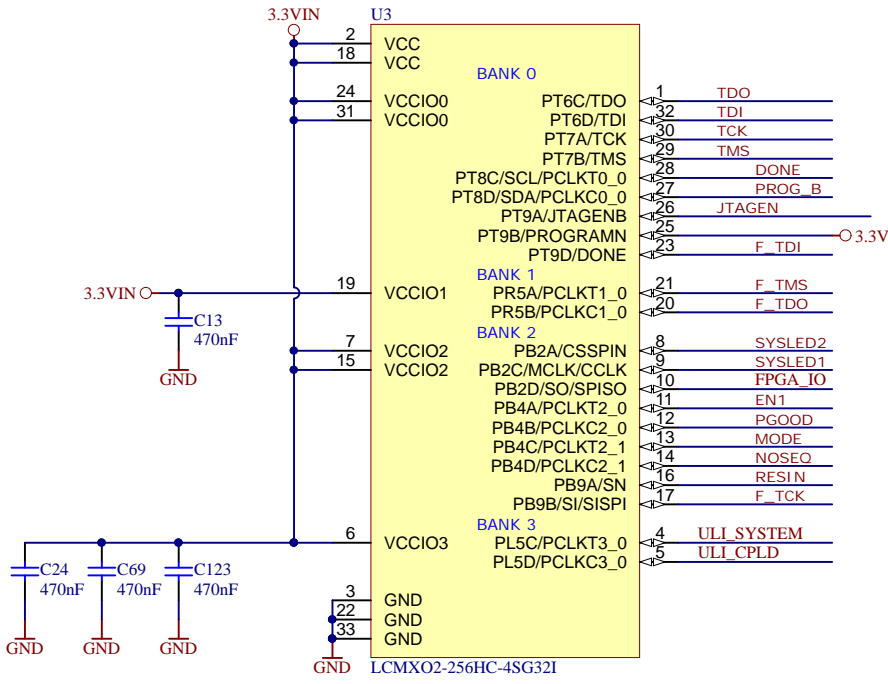
trenz electronic

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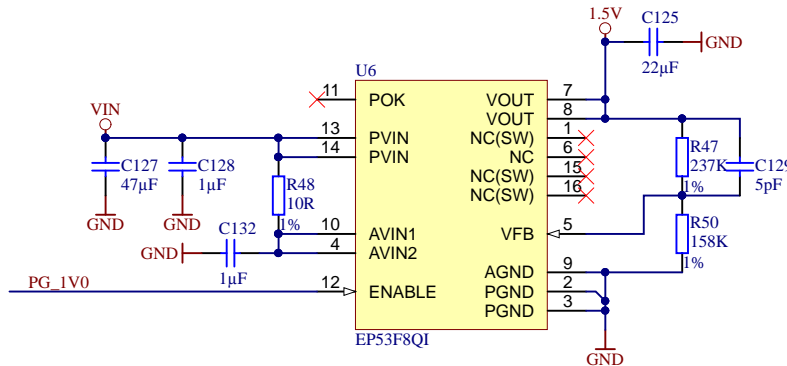
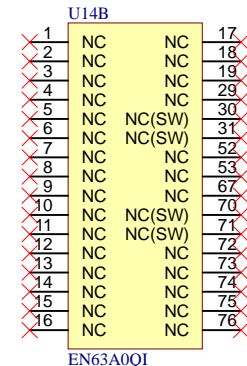
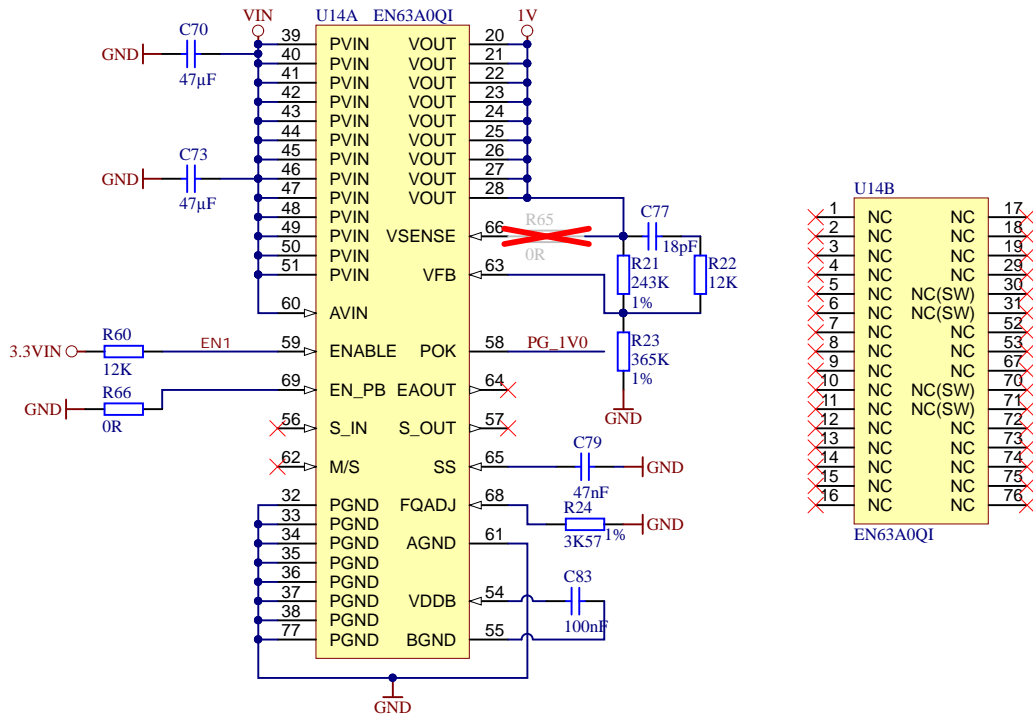
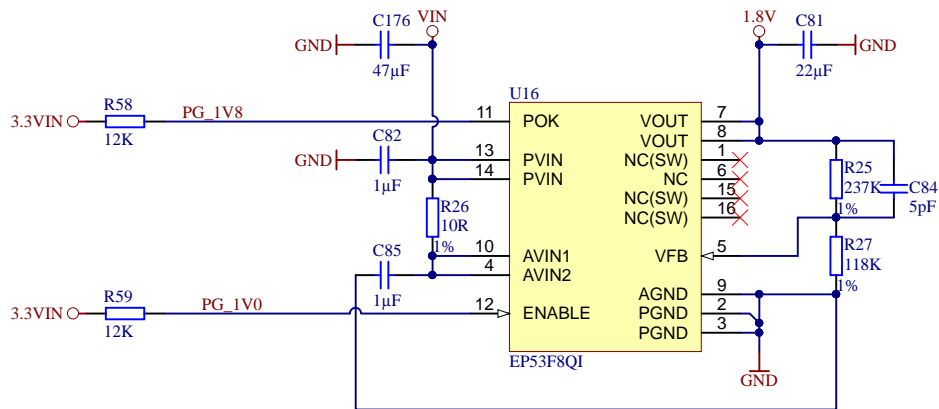
A4	Number: TE0712 35-21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 12 of 16
Filename: DDR3-RAM.SchDoc		



	Title: ETH		
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	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
	Page 13 of 16		Filename: ETHERNET.SchDoc

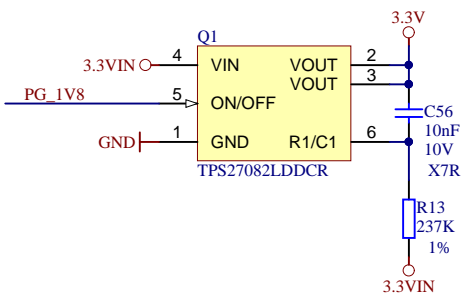


Title: CPLD		
A4	Number: TE0712 35-21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 14 of 16
Filename: CPLD.SchDoc		



R65 R66 MODE EN63A0QI

OK	X	enable pre-bias start-up
X	OK	disable pre-bias start-up



- VIN ○ TP1 ● Testpoint 0.8mm
- 1V ○ TP2 ● Testpoint 0.8mm
- GND TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP5 ● Testpoint 0.8mm
- GND TP9 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- GND TP12 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- GND TP15 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm
- GND TP16 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm



Title: PWR		
A4	Number: TE0712 35-21	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 15 of 16
Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

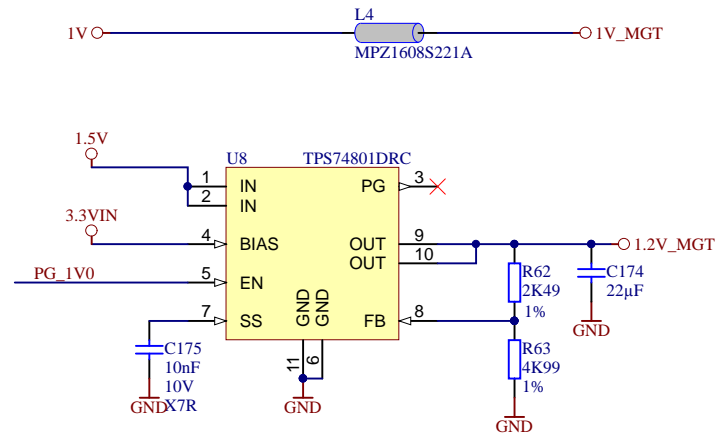
B


C

C

D

D



	Title: PWR		
	A4	Number: TE0712 35-2I	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 16 of 16
	Filename: PWR2.SchDoc		

1

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