VIPER122

High voltage converter

Datasheet - production data

Features

- 730 V avalanche rugged power MOSFET
- PWM controller
- 3.3 V reference voltage
- Frequency jittering
- 40 mW no load input power at 230 V_{AC}
- Short-circuit protection
- Thermal shutdown

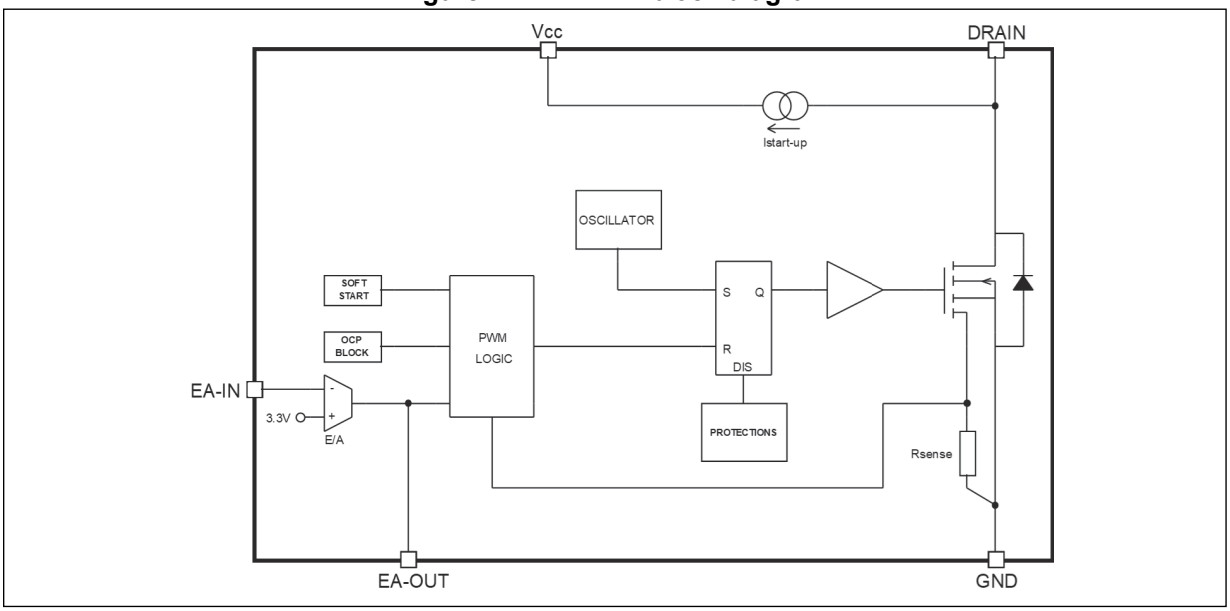
Applications

- Auxiliary SMPS for:
  - home appliances
  - consumer goods
  - industrial
  - lighting

Description

The device is a high performance high voltage converter that combines a 730 V rugged power MOSFET with PWM control. The device embeds high voltage startup and current sense circuitry, which helps reduce the number of components in a BoM. Frequency jittering spreads the EMI and allows the use of a smaller filter. The burst mode feature provides very low input power consumption at light loads.

Figure 1. VIPER122 block diagram



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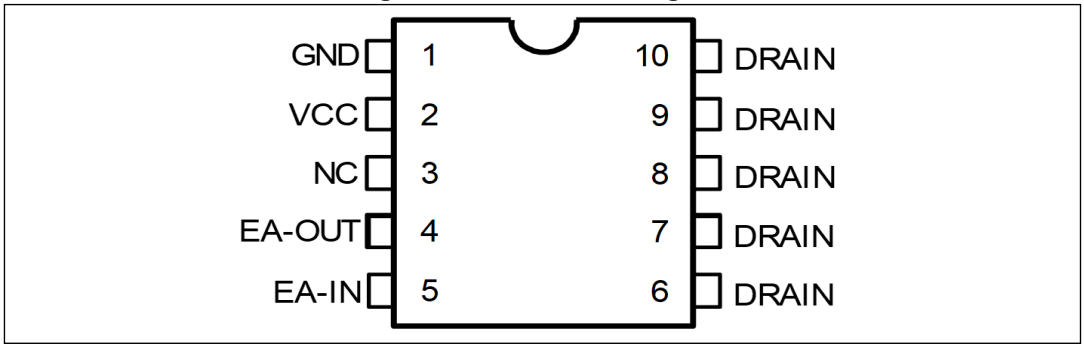


Table 1. Pin descriptions

SSOP10	Name	Function
1	GND	Connected to the source of the internal power MOSFET and controller ground reference.
2	VCC	Supply voltage of the control section. This pin provides the charging current of the external capacitor.
3	NC	Not connected. The pin must be left floating.
4	EA-OUT	Output of the error amplifier.
5	EA-IN	Input of the error amplifier.
6-10	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Connect to a PCB copper area to facilitate heat dissipation.

2 Typical power capability

Table 2. Typical power

V_{IN}: 230 V_{AC}		V_{IN}: 85 - 265 V_{AC}	
Adapter[1]	Open frame[2]	Adapter[1]	Open frame[2]
9 W	11 W	5 W	6 W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient temperature.
2. Maximum practical continuous power in an open frame design at 50 °C ambient temperature, with adequate heat-sinking.

3 Electrical and thermal ratings

Table 3. Absolute maximum rating

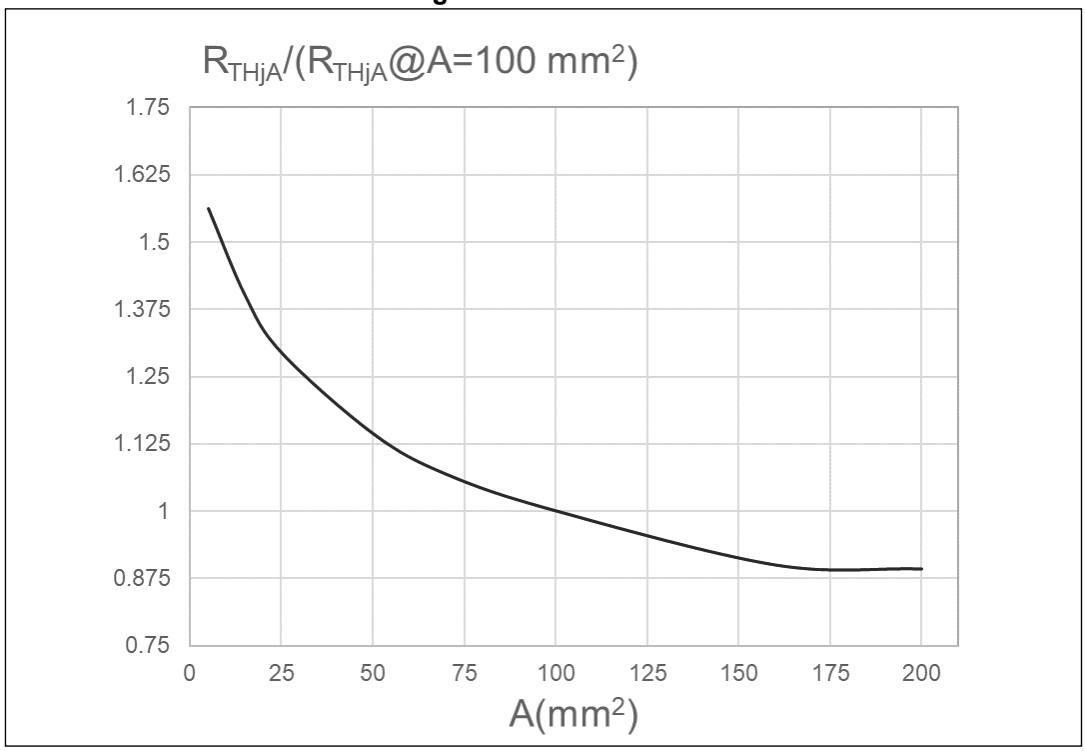
Symbol	Pin	Parameter	Value		Unit
			Min.	Max.	
V_{DS}	6-10	Drain-to-source (ground) voltage	-	730	V
I_D	6-10	Pulse drain current (limited by T_J = 150 °C)	-	2	A
V_{EA-IN}	5	Input pin voltage	-0.3	4.8	V
V_{EA-OUT}	4	Out pin voltage	-0.3	3.5	V
V_{CC}	2	Supply voltage	-0.3	Self limited	V
I_{CC}	2	Input current	-	20	mA
P_{TOT}	-	Power dissipation at T_A < 50 °C	-	1	W
T_J	-	Junction temperature range	-40	150	°C
T_{STG}	-	Storage temperature	-55	150	°C

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
R_{TH-JC}	Thermal resistance junction to case(1) (Dissipated power = 1 W)	10	°C/W
R_{TH-JA}	Thermal resistance junction ambient(1) (Dissipated power = 1 W)	155	°C/W
R_{TH-JC}	Thermal resistance junction to case(2) (Dissipated power = 1 W)	5	°C/W
R_{TH-JA}	Thermal resistance junction ambient(2) (Dissipated power = 1 W)	95	°C/W

1. When mounted on a standard single side FR4 board with minimum copper area.
2. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq in) of Cu (35 µm thick).

Figure 3. Rth vs. area



4 Electrical characteristics

(T_J = 25 °C, V_{CC} = 14 V, unless otherwise specified.)

Table 5. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_D = 1 mA, EA-OUT = GND	730	-	-	V
$R_{DS(on)}$	Drain-source ON state resistance	I_D = 0.2 A; T_J = 25 °C	-	-	27	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 100 V(1)	-	12	-	pF
I_{DSS}	OFF state DRAIN leakage current	V_{DRAIN} = 730 V	-	-	70	µA
V_{START}	Drain-source start voltage	-	-	-	45	V
I_{CH1}	Startup charging current	V_{DRAIN} = 100 V V_{CC} = 4 V	-0.6	-	-1.8	mA
I_{CH2}	Charging current during operation	V_{DRAIN} = 100 V V_{CC} = 9 V falling edge	-7	-	-14	mA
V_{CC}	Operating voltage range	-	11.5	-	23.5	V
V_{CLAMP}	V_{CC} clamp voltage	I_{CC} = 15 mA	23.5	-		V
V_{ON}	V_{CC} ON threshold	-	12	13	14	V
V_{CCL}	V_{CC} low value	-	9.5	10.5	11.5	V
V_{OFF}	UVLO	-	7	8	9	V
I_{CC0}	Operating supply current, not switching	Not switching	-	-	0.7	mA
I_{CC1}	Operating supply current, switching	Switching	-	-	1.6	mA
I_{CC2}	Operating supply current, with $V_{CC} < V_{OFF}$	V_{CC} = 6 V	-	-	0.35	mA
I_{CC_FAIL}	VCC clamp protection	$V_{CC} = V_{CLAMP}$ V_{EA-OUT} = 3.3 V	4	-	-	mA
I_{LIM}	Drain current limit (OCP)	V_{EA-OUT} = 3.3 V	0.4	0.45	0.5	A
$T_{ON(MIN)}$	Minimum turn ON time	-	-	-	450	ns
F_{OSC}	-	-	54	60	66	kHz
F_D	Modulation depth	-	-	±4	-	kHz
F_M	Modulation frequency	-	-	230	-	Hz
D_{MAX}	Max. duty cycle	(1)	70	-	80	%
V_{REF}	E/A reference voltage	-	3.2	3.3	3.4	V
$I_{PULL\ UP}$	EA-IN pin current pull up	-	-	-1	-	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_M	E/A Trans conductance	(1)	-	2	-	mA/V
V_{EA-SAT}	EA-OUT pin saturation limit	-	-	3	-	V
V_{EA-BM}	Burst mode threshold	-	1	1.1	1.2	V
V_{HYST}	Burst mode hysteresis	-	-	40	-	mV
R_{DYN}	Dynamic resistance	V_{EA-IN} = GND	-	15	-	kΩ
H_{EA-OUT}	$\Delta V_{EA-OUT} / \Delta I_D$	(1)	3	-	6	V/A
I_{EA-OUT}	EA-OUT pin source / sink current	-	-	150	-	µA
I_{EA-OUT_MAX}	EA-OUT pin max. source current	-	-	220	-	µA
T_{SD}	Thermal shutdown temperature	(1)	150	160	-	°C
T_{HYST}	Thermal shutdown hysteresis	(1)	-	30	-	°C

1. Specification assured by characterization.

5 Typical electrical characteristics

Figure 4. I_{LIM} vs. T_J

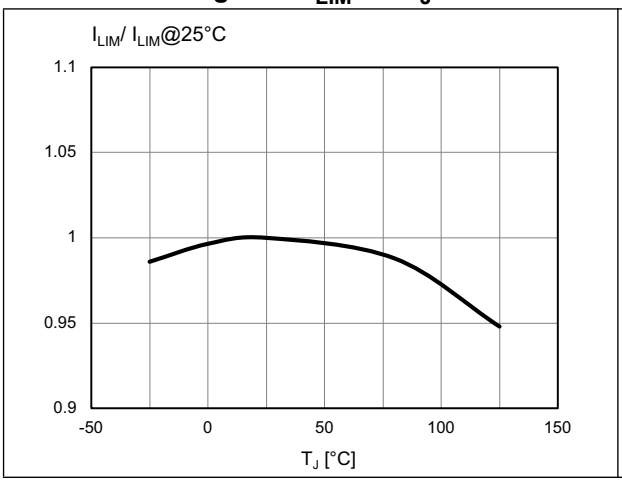


Figure 5. V_{REF} vs. T_J

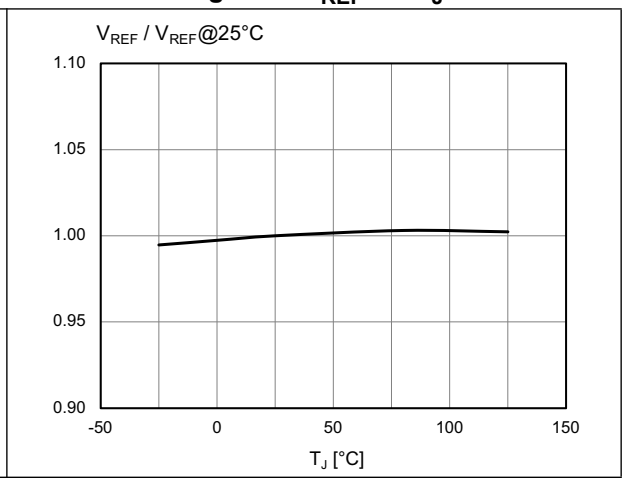


Figure 6. I_{CC0} vs. T_J

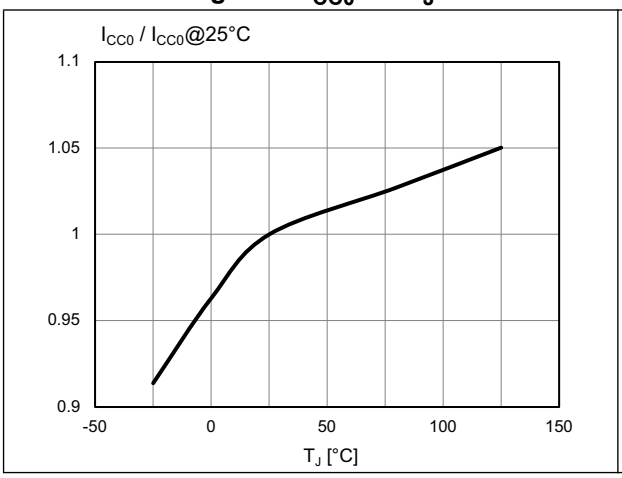


Figure 7. I_{CC1} vs. T_J

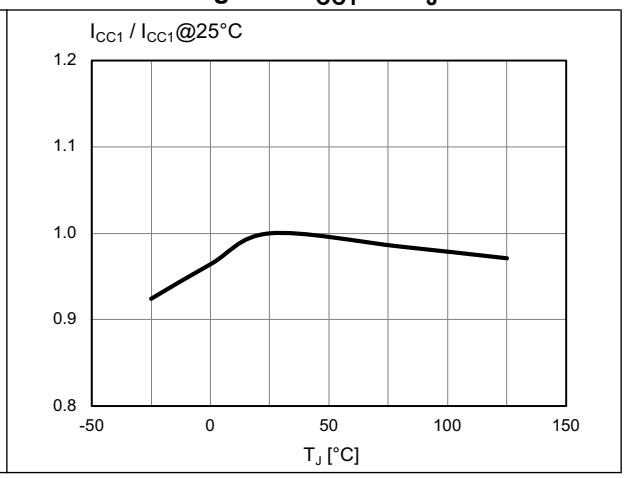


Figure 8. $R_{DS(on)}$ vs. T_J

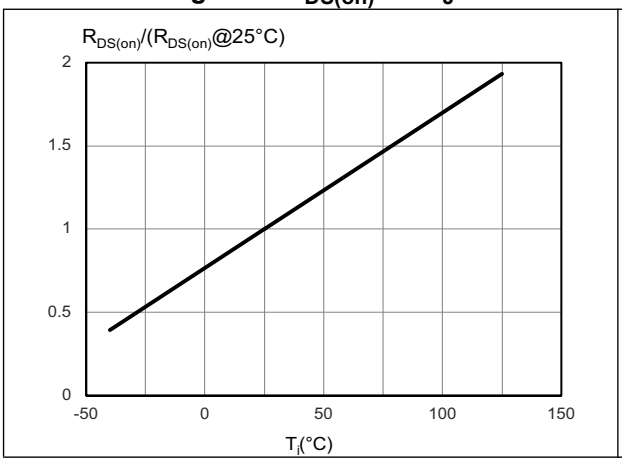
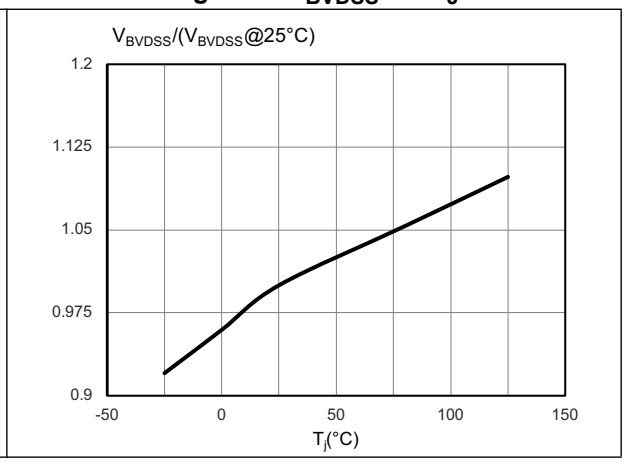


Figure 9. V_{BVDSS} vs. T_J



6 General description

The VIPER122 is a 730 V high voltage converter optimized for flyback and buck topologies that operates at 60 kHz switching frequency and integrates jittering in order to reduce EMI levels.

The low IC consumption combined with Burst Mode allows very low input power at no load and very good efficiency at light load.

6.1 Startup

On initial startup, the integrated high voltage current source charges the VCC capacitor. The charge current I_{CH1} is stopped as soon as the VCC voltage reaches V_{ON}.

As soon as the VCC capacitor is charged up to the V_{ON} threshold, the power MOSFET starts switching in soft-start mode and the device is either supplied from an external source (auxiliary winding or directly from the output voltage through a diode) or internally from the high voltage startup that is reactivated whenever the VCC voltage drops to the VCCL level.

Soft-start is staggered over 16 steps up to the default current limit value (I_{LIM}), over a period of 8.5 ms.

In case of fault detection, the VCC voltage moves between V_{ON} (13 V) and V_{CCL} (10.5 V) and power MOSFET switching is only interrupted if the VCC voltage falls below the UVLO (V_{OFF}) threshold, which typically occurs if the DRAIN voltage is removed.

6.2 Feedback loop

The device operates in current mode, so the primary current is internally sensed and converted into voltage that is applied to the non-inverting pin of the PWM comparator. The sensed voltage is compared through a voltage divider on a cycle-by-cycle basis with the voltage on the EA-IN pin.

The OCP comparator works in parallel with the PWM comparator and limits the primary current below the I_{LIM} threshold.

There are two ways to close the loop and regulate the output: through a resistor divider or an optocoupler.

6.2.1 Resistor divider

For non-isolated topologies (flyback, buck or buck-boost converters), the output voltage can be directly regulated by connecting a resistor divider to the EA-IN pin that is the inverting input of the integrated error amplifier (EA).

Primary side regulation can be achieved by connecting the resistor divider from the auxiliary winding of the transformer to the EA-IN pin.

The loop compensation network is connected on the EA-OUT pin.

6.2.2 Optocoupler

For an isolated flyback, the EA-IN pin must be connected to ground and the optocoupler connected to the EA-OUT pin.

The EA-OUT pin dynamics range between the values V_{EA-SAT} and V_{EA-BM}: above the V_{EA-SAT} level, the primary drain current reaches its limit; below the V_{EA-BM} level, the device enters Burst Mode.

6.3 Burst mode at light load

When the load decreases, the feedback loop reacts by lowering the EA-OUT pin voltage. If it falls below the V_{EA-BM} threshold, power MOSFET switching is interrupted until it returns above V_{EA-BM} + V_{HYST}.

During Burst Mode, the drain current peak is clamped to about 85 mA in order to avoid audible noise due to the low switching frequency.

6.4 Short-circuit protection

The protection for a short-circuit is only tripped if the event persists for 50 ms If the protection is tripped, the device stops switching for 1 second and then restarts automatically.

6.5 VCC clamp protection

A fault condition is detected if both of the following conditions are verified:

1. The primary drain current reaches the I_{LIM} threshold value.
2. The clamp current injected on the VCC pin reaches the I_{CC_FAIL} threshold value.

When the protection is tripped, the device stops switching for 1 second and then restarts automatically. The device is protected in case of failure of the feedback network.

7 Basic application schematics

Figure 10. Non-isolated flyback converter

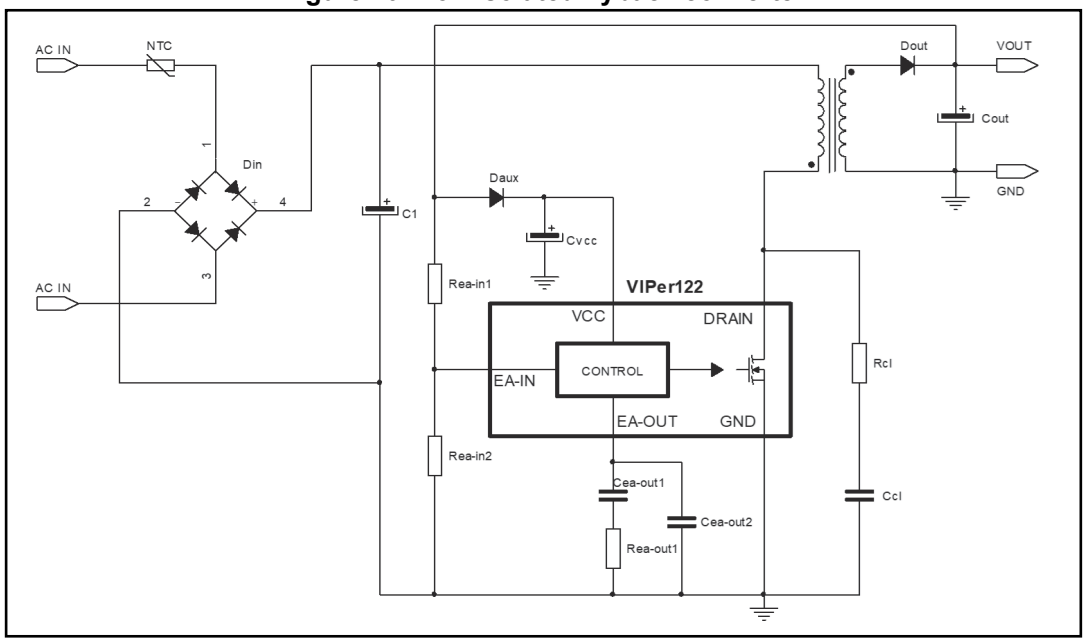


Figure 11. Primary side flyback converter

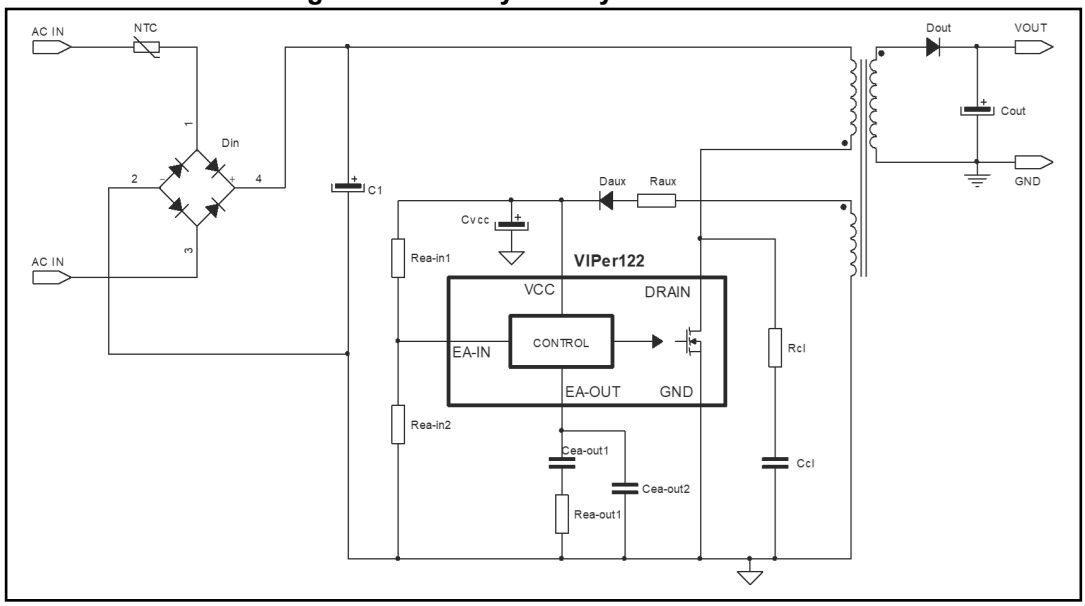


Figure 12. Isolated flyback converter

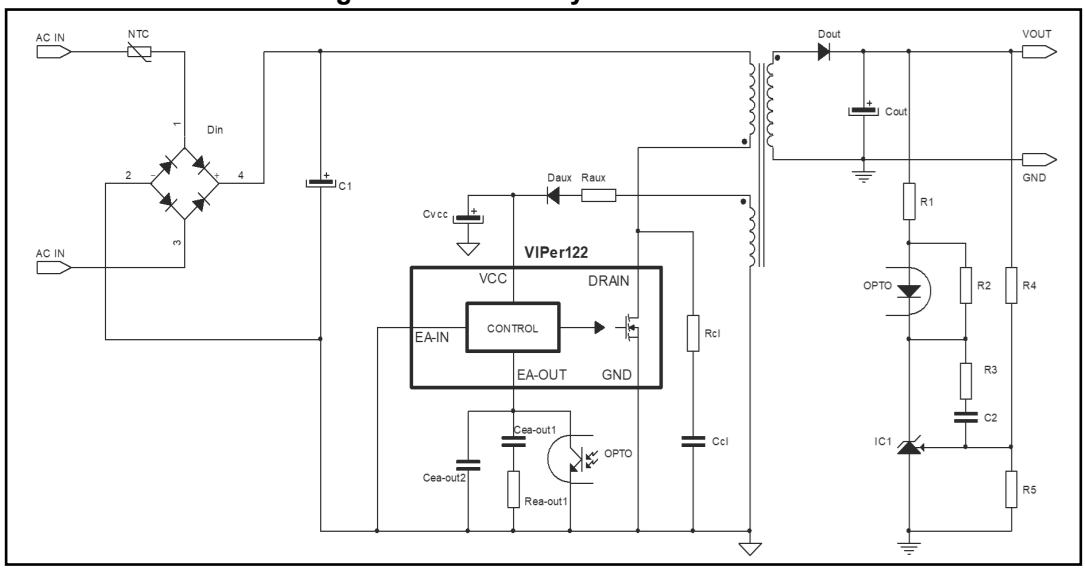


Figure 13. Buck converter

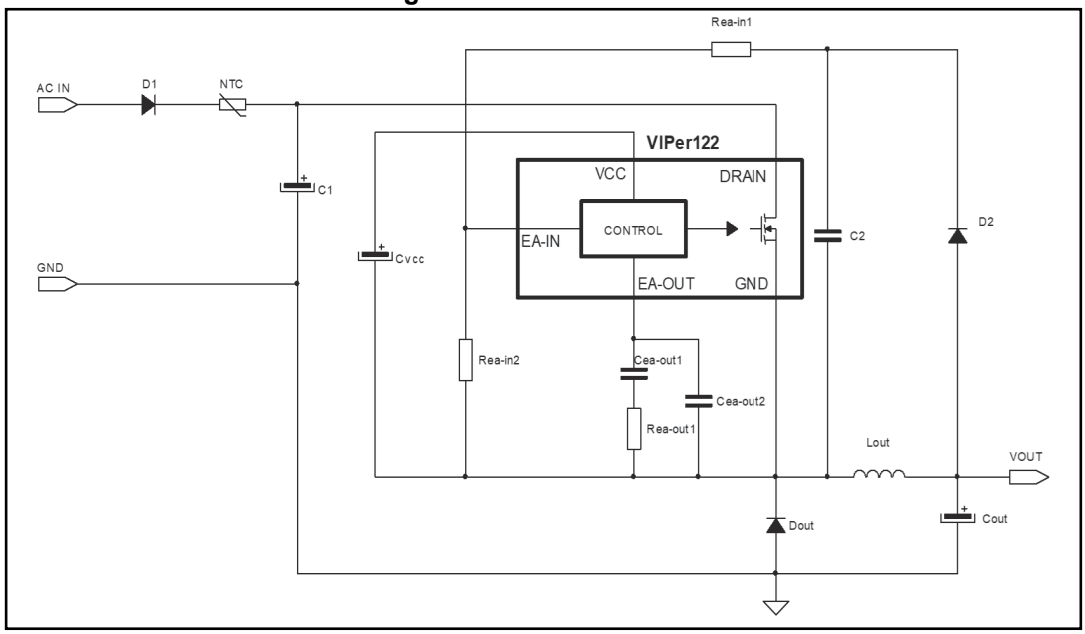
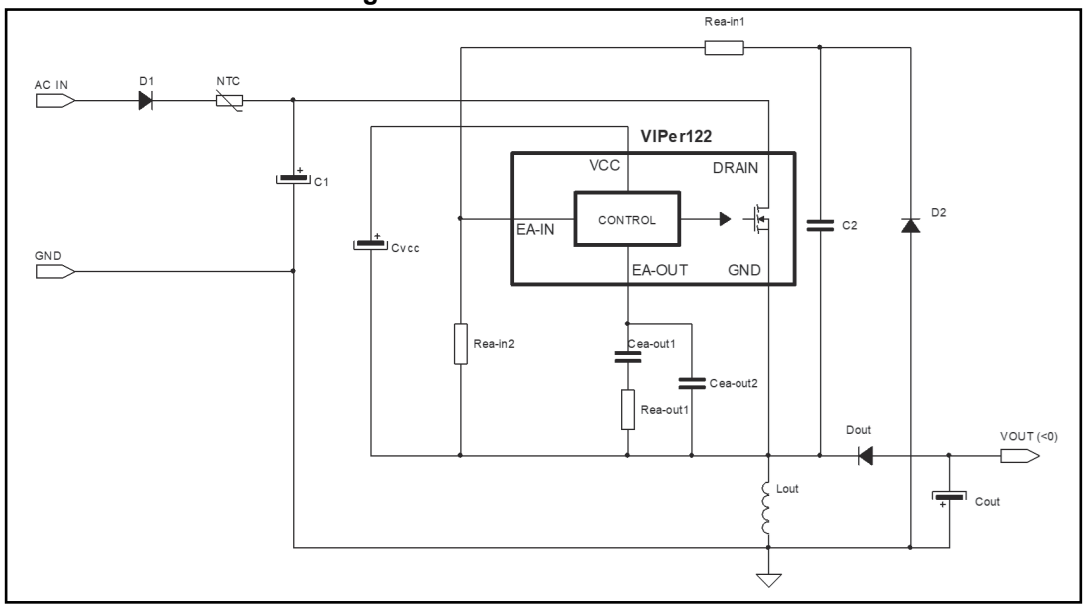


Figure 14. Buck-boost converter



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 SSOP10 package information

Figure 15. SSOP10 package outline

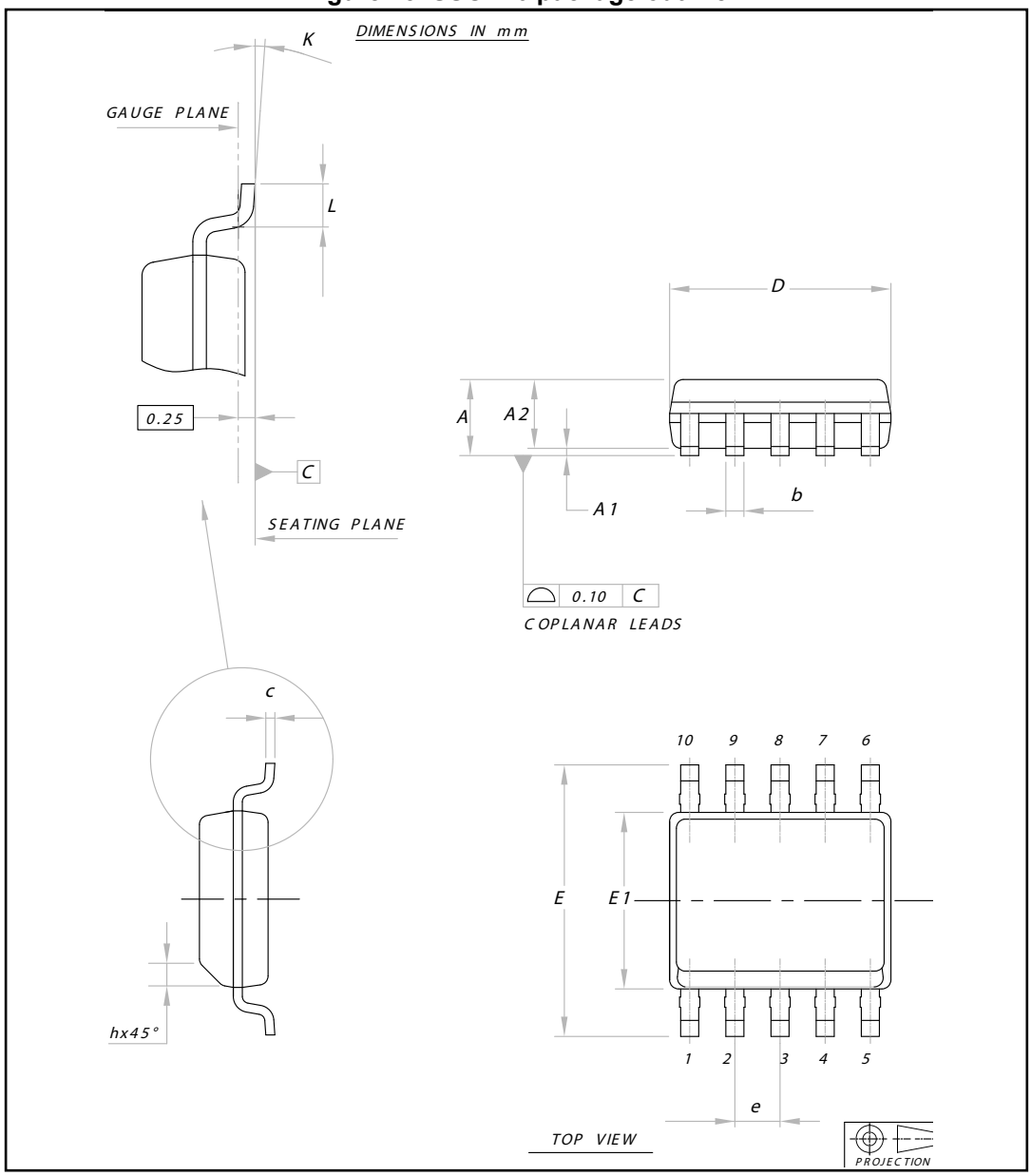
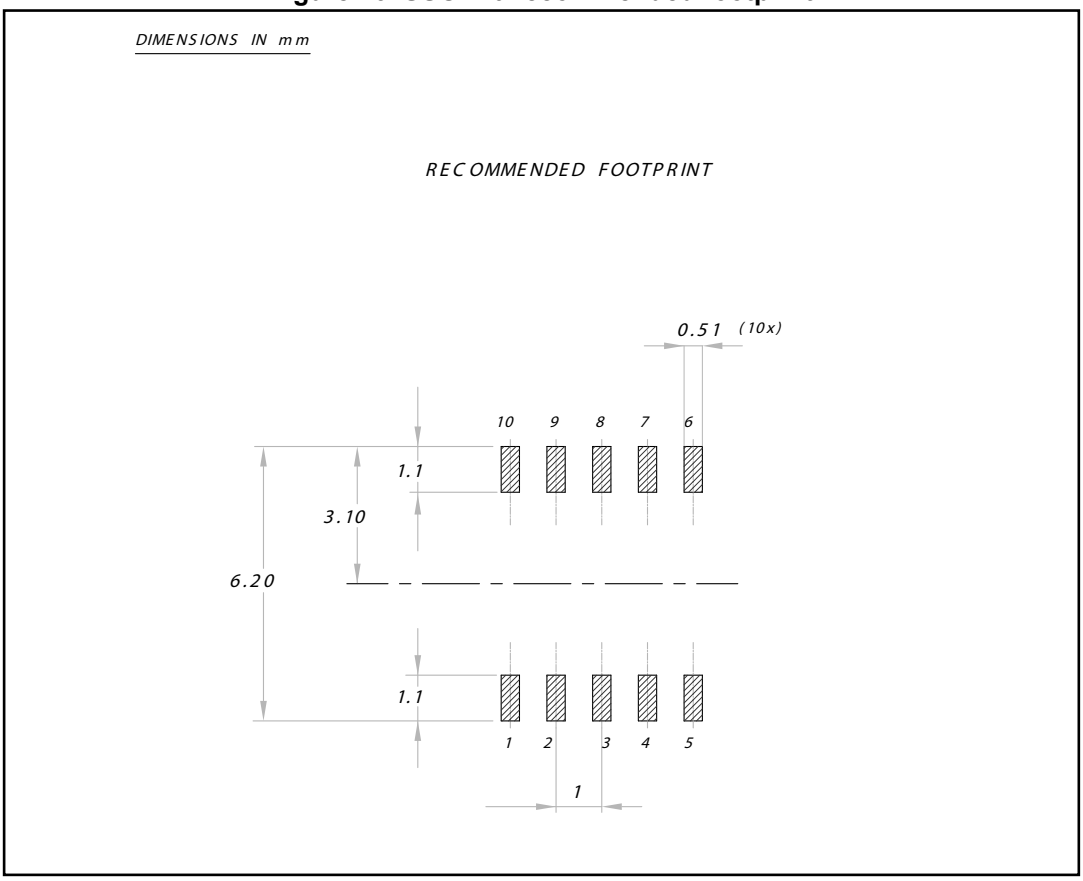


Table 6. SSOP10 mechanical data

Dim	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e		1	
h	0.25		0.50
L	0.40		0.90
K	0°		8°

Figure 16. SSOP10 recommended footprint



9 Ordering information

Table 7. Order code

Order code	Package	Packaging
VIPER122LSTR	SSOP10	Tape & Reel

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
4-Jun-2019	1	Initial release.

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