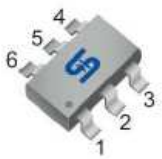
TSM3911D

20V Dual P-Channel MOSFET

SOT-26



Pin Definition:

1. Gate 1
2. Source 2
3. Gate 2
6. Drain 1
5. Source 1
4. Drain 2

Key Parameter Performance

Parameter		Value	Unit
V_{DS}		-20	V
$R_{DS(on)}$ (max)	V_{GS} = -4.5V	140	mΩ
	V_{GS} = -2.5V	200	
	V_{GS} = -1.8V	300	
Q_g		15.23	nC

Features

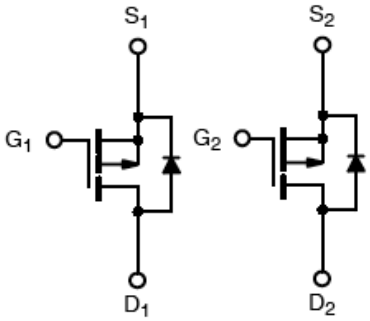
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Ordering Information

Part No.	Package	Packing
TSM3911DCX6 RFG	SOT-26	3kpcs / 7" Reel

Note: "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

Block Diagram



Dual P-Channel MOSFET

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current		I_D	-2.2	A
Pulsed Drain Current		I_{DM}	-8	A
Continuous Source Current (Diode Conduction) (Note 1,2)		I_S	-0.72	A
Maximum Power Dissipation	T_A= 25°C	P_D	1.15	W
	T_A=70°C		0.73	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JC}$	30	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	80	°C/W

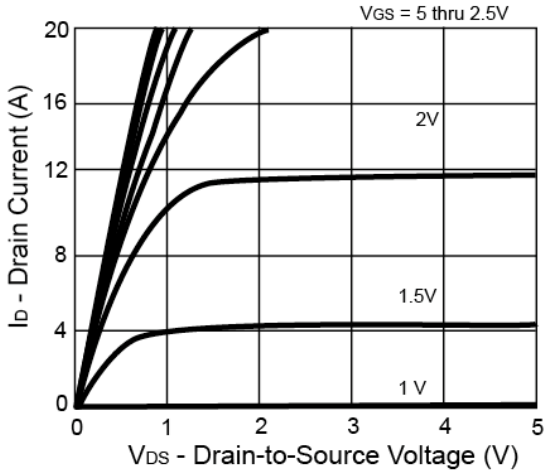
Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static (Note 3)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-0.45	--	-0.95	V
Gate Body Leakage	V_{GS} = ±8V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	μA
On-State Drain Current	V_{DS} =-5V, V_{GS} = -5V	$I_{D(ON)}$	-5	--	--	A
Drain-Source On-State Resistance	V_{GS} = -4.5V, I_D = -2.2A	$R_{DS(ON)}$	--	115	140	mΩ
	V_{GS} = -2.5V, I_D = -1.8A		--	163	200	
	V_{GS} = -1.8V, I_D = -1A		--	220	300	
Forward Transconductance	V_{DS} = -5V, I_D = -2.2A	g_{fs}	--	5	--	S
Diode Forward Voltage	I_S = -1.05A, V_{GS} = 0V	V_{SD}	--	- 0.8	-1.2	V
Dynamic (Note 4)						
Total Gate Charge	V_{DS} = -6V, I_D = -2.8A, V_{GS} = -4.5V	Q_g	--	15.23	--	nC
Gate-Source Charge		Q_{gs}	--	5.49	--	
Gate-Drain Charge		Q_{gd}	--	2.74	--	
Input Capacitance	V_{DS} = -6V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	882.51	--	pF
Output Capacitance		C_{oss}	--	145.54	--	
Reverse Transfer Capacitance		C_{rss}	--	97.26	--	
Switching (Note 4,5)						
Turn-On Delay Time	V_{DD} = -6V, R_L = 6Ω, I_D = -1A, V_{GEN} = -4.5V, R_G = 6Ω	$t_{d(on)}$	--	17.28	--	ns
Turn-On Rise Time		t_r	--	3.73	--	
Turn-Off Delay Time		$t_{d(off)}$	--	36.05	--	
Turn-Off Fall Time		t_f	--	6.19	--	

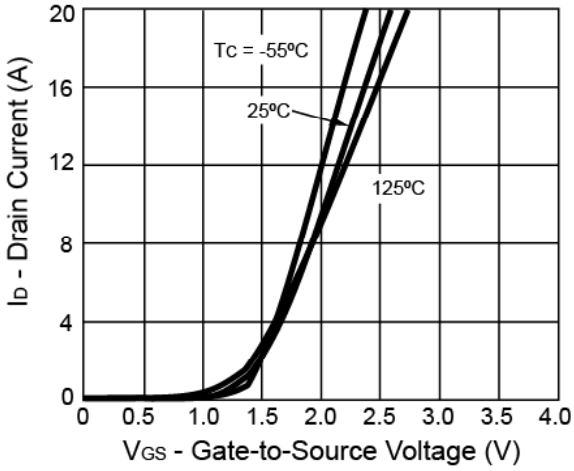
Notes:
1. Pulse width limited by the Maximum junction temperature
2. Surface Mounted on FR4 Board, t ≤ 5 sec.
3. pulse test: PW ≤ 300μS, duty cycle ≤ 2%
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

Electrical Characteristics Curves

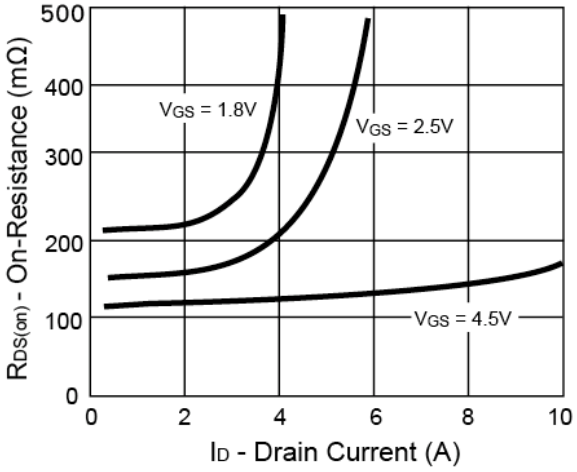
Output Characteristics



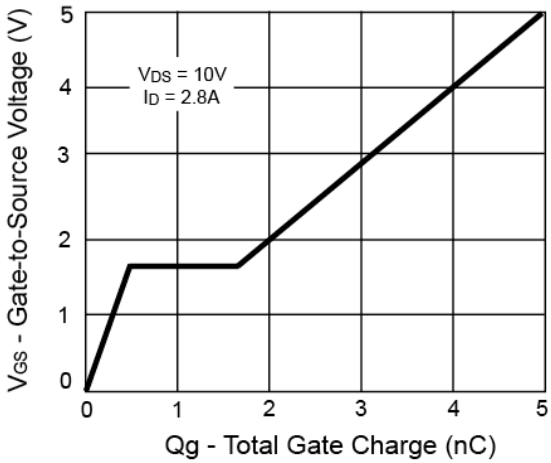
Transfer Characteristics



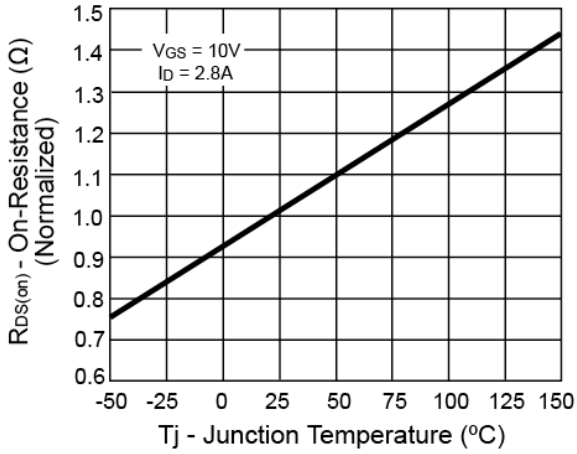
On-Resistance vs. Drain Current



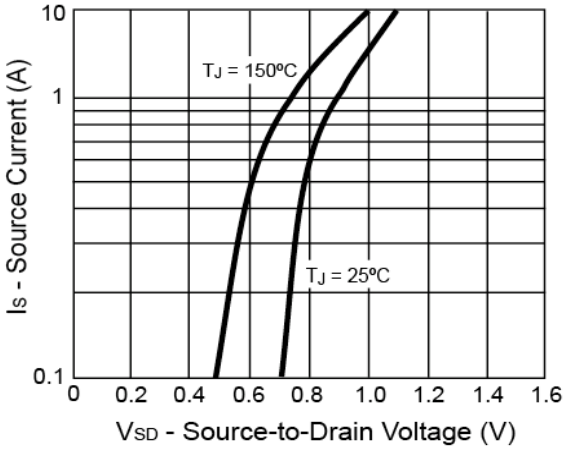
Gate Charge



On-Resistance vs. Junction Temperature

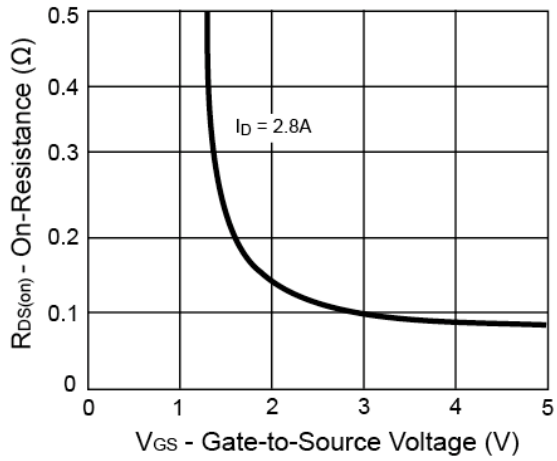


Source-Drain Diode Forward Voltage

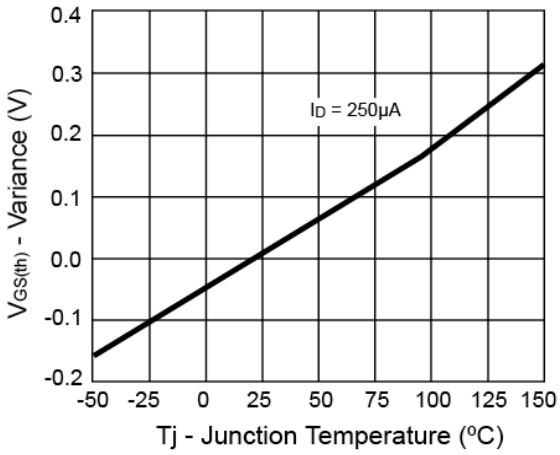


Electrical Characteristics Curves

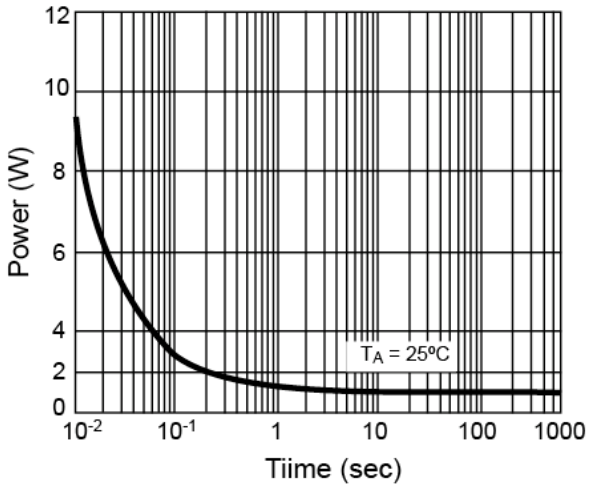
On-Resistance vs. Gate-Source Voltage



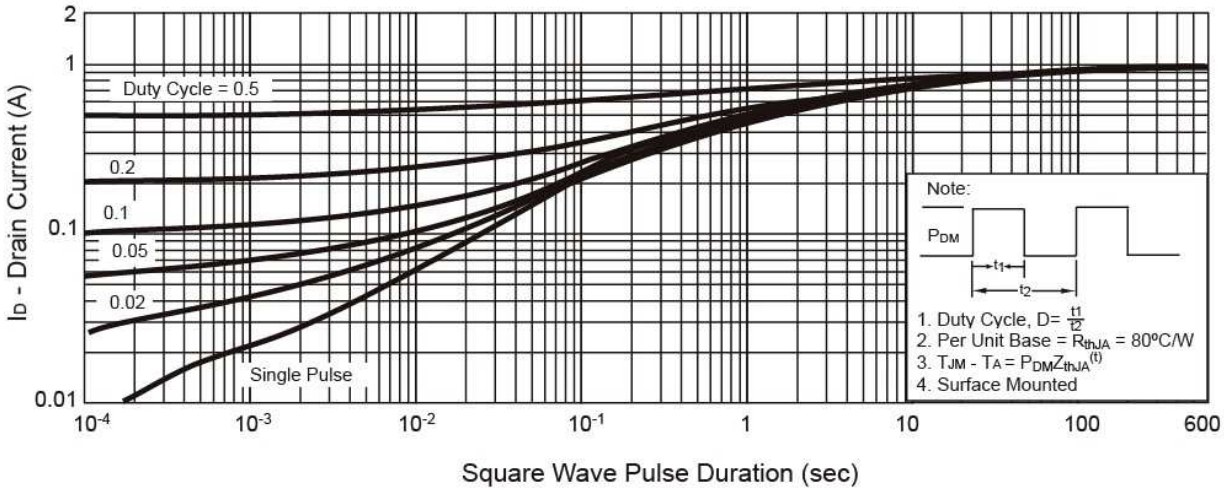
Threshold Voltage



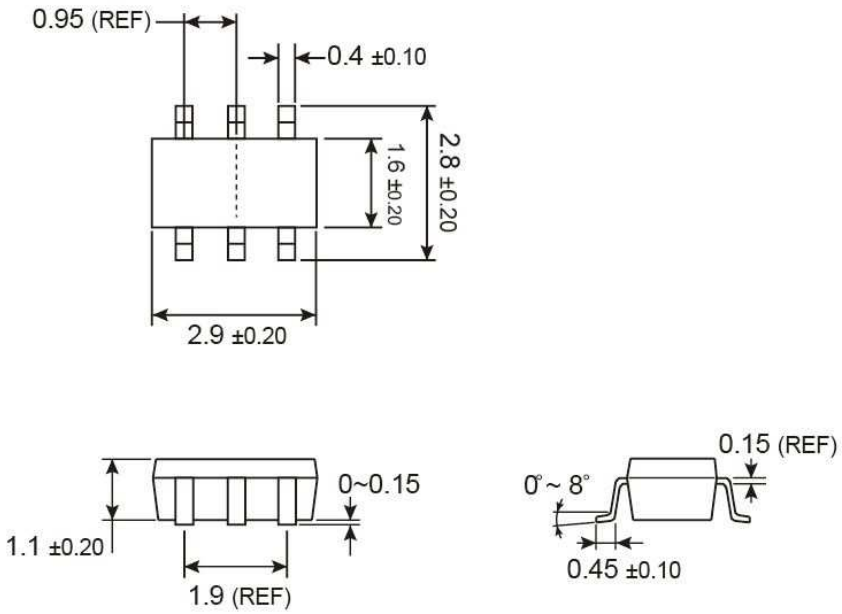
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

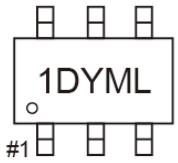


SOT-26 Mechanical Drawing



Unit: Millimeters

Marking Diagram



1D = Device Code
Y = Year Code
M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code

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