# NBSG72A

# 2.5V/3.3V SiGe Differential 2 X 2 Crosspoint Switch with Output Level Select

The NBSG72A is a high−bandwidth fully differential 2 X 2 crosspoint switch with Output Level Select (OLS) capabilities. This is a part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a low profile 3 X 3 mm 16−pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The OLS input is used to program the peak−to−peak output amplitude between 0 mV and 800 mV in five discrete steps. The SELECT inputs are single−ended and can be driven with either LVECL or LVCMOS/LVTTL input levels.

- Maximum Input Clock Frequency > 7 GHz Typical
- Maximum Input Data Rate > 7 Gb/s Typical
- 200 ps Typical Propagation Delay (OLS = FLOAT)
- 55/45 ps Typical Rise/Fall Times (OLS = FLOAT)
- Selectable Swing PECL Output with Operating Range: $V_{CC}$ = 2.375 V to 3.465 V with $V_{EE}$ = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = −2.375 V to −3.465 V
- Selectable Output Levels (0 mV, 200 mV, 400 mV, 600 mV or 800 mV Peak−to−Peak Output)
- 50 Ω Internal Input Termination Resistors
- Single−Ended LVECL or LVCMOS/LVTTL Select Inputs (SELA, SELB)
- Pb−Free Package is Available

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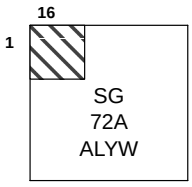
**MARKING DIAGRAM***


**QFN−16**
**MN SUFFIX**
**CASE 485G**




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |

*For additional marking information, refer to Application Note AND8002/D.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

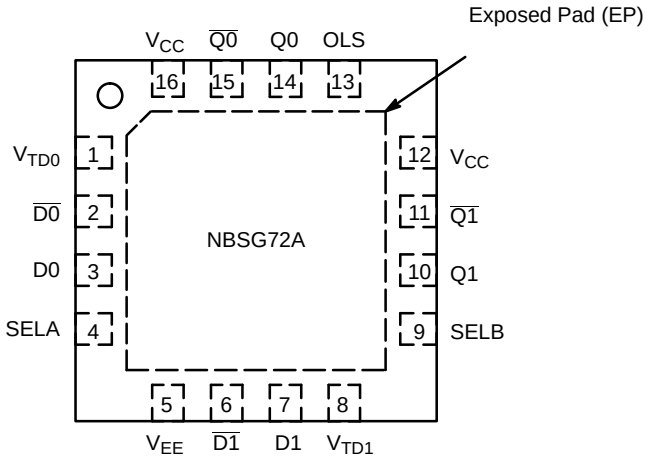



**Figure 1. QFN−16 Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| 1 | VTD0 | − | Common Internal 50 Ω Termination Pin for D0 and $\overline{D0}$ Input. See Table 4. (Note 1) |
| 2 | $\overline{D0}$ | LVDS, CML, ECL, LVTTL, LVCMOS Input | Inverted Differential Input 0. |
| 3 | D0 | LVDS, CML, ECL, LVTTL, LVCMOS Input | Noninverted Differential Input 0. |
| 4 | SELA | LVECL, LVCMOS Input | Select Logic Input A. Internal 75 kΩ Pulldown to $V_{EE}$. |
| 5 | $V_{EE}$ | − | Negative Supply. All $V_{EE}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| 6 | $\overline{D1}$ | LVDS, CML, ECL, LVTTL, LVCMOS Input | Inverted Differential Input 1. |
| 7 | D1 | LVDS, CML, ECL, LVTTL, LVCMOS Input | Noninverted Differential Input 1. |
| 8 | VTD1 | − | Common Internal 50 Ω Termination Pin for D1 and $\overline{D1}$ Input. See Table 4. (Note 1) |
| 9 | SELB | LVECL, LVCMOS Input | Select Logic Input B. Internal 75 kΩ Pulldown to $V_{EE}$. |
| 10 | Q1 | RSECL Output | Noninverted Differential Output. |
| 11 | $\overline{Q1}$ | RSECL Output | Inverted Differential Output. |
| 12 | $V_{CC}$ | − | Positive Supply. All $V_{CC}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| 13 | OLS (Note 2) | Input | Input Pin for Output Level Select (OLS) See Table 3. |
| 14 | Q0 | RSECL Output | Noninverted Differential Output Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2.0$ V. |
| 15 | $\overline{Q0}$ | RSECL Output | Inverted Differential Output Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2.0$ V. |
| 16 | $V_{CC}$ | − | Positive Supply. All $V_{CC}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| − | EP | − | Exposed Pad. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat−sinking conduit. |

1. In the differential configuration when the input termination pins (VTD0, VTD1) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self−oscillation.
2. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2 kΩ resistor should be connected from OLS pin to $V_{EE}$.

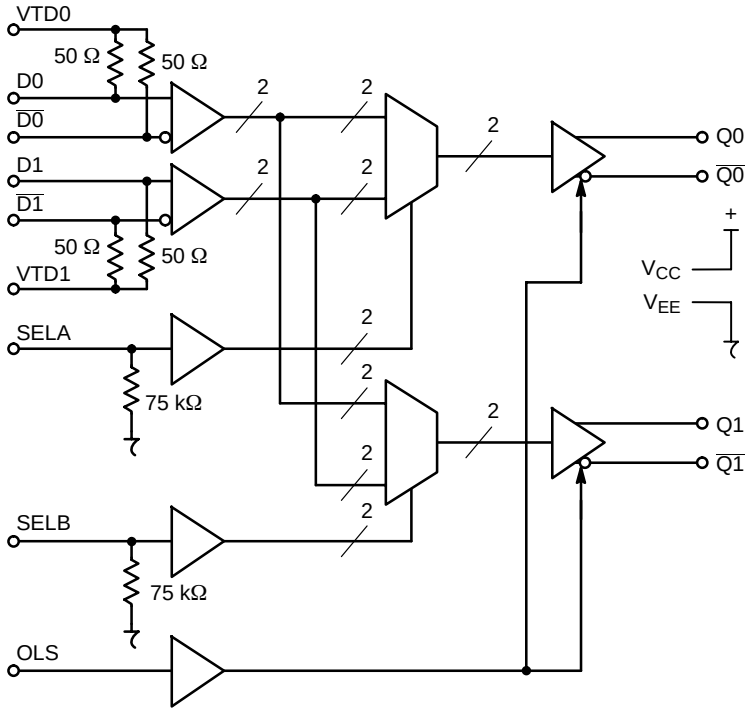



**Figure 2. Logic/Block Diagram**

**Table 2. TRUTH TABLE**

| SELA | SELB | Q0 | Q1 |
|---|---|---|---|
| LOW | LOW | D0 | D0 |
| HIGH | LOW | D1 | D0 |
| LOW | HIGH | D0 | D1 |
| HIGH | HIGH | D1 | D1 |

**Table 3. OUTPUT LEVEL SELECT (OLS)**

| OLS | Output Amplitude ($V_{OUTPP}$) | OLS Sensitivity |
|---|---|---|
| $V_{CC}$ | 800 mV | OLS − 75 mV |
| $V_{CC}$ − 0.4 V | 200 mV | OLS ± 150 mV |
| $V_{CC}$ − 0.8 V | 600 mV | OLS ± 100 mV |
| $V_{CC}$ − 1.2 V | 0 | OLS ± 75 mV |
| $V_{EE}$ (Note 3) | 400 mV | OLS ± 100 mV |
| FLOAT | 600 mV | N/A |

3. When an output level of 400 mV is desired and $V_{CC}$ − $V_{EE}$ > 3.0 V, a 2 kΩ resistor should be connected from OLS to $V_{EE}$.

**Table 4. INTERFACING OPTIONS**

| Interfacing Options | Connections |
|---|---|
| CML | Connect VTD0 and VTD1 to $V_{CC}$ |
| LVDS | VTD0 and VTD1 Should Be Left Floating. |
| AC−COUPLED | Bias VTD0 and VTD1 Inputs within Common Mode Range (VIHCMR) |
| RSECL, PECL, NECL | Standard ECL Termination Techniques |
| LVCMOS / LVTTL | The external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTL and $V_{CC}$/2 for LVCMOS Inputs. |

**Table 5. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor (SELA, SELB) | | 75 kΩ |
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 50 V<br>> 1 kV |
| Moisture Sensitivity (Note 1) | | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 436 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, see Application Note AND8003/D.

**Table 6. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | $V_{EE}$ = 0 V | | 3.6 | V |
| $V_{EE}$ | Negative Power Supply | $V_{CC}$ = 0 V | | −3.6 | V |
| $V_I$ | Positive Input<br>Negative Input | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 3.6<br>−3.6 | V<br>V |
| $V_{INPP}$ | Differential Input Voltage $\|D_X - \overline{D_X}\|$ | $V_{EE} - V_{CC} \geq$ 2.8 V<br>$V_{EE} - V_{CC} <$ 2.8 V | | 2.8<br>$\|V_{CC} - V_{EE}\|$ | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 25<br>50 | mA<br>mA |
| $I_{IN}$ | Input Current Through $R_T$ (50 Ω Resistor) | Static<br>Surge | | 45<br>80 | mA<br>mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 2) | 0 lfpm<br>500 lfpm | QFN−16<br>QFN−16 | 42<br>35 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | (Note 2) | QFN−16 | 4 | °C/W |
| $T_{sol}$ | Wave Solder | < 15 sec | | 225 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 1S2P (1 signal, 2 power).

**Table 7. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT** $V_{CC}$ = 2.5 V; $V_{EE}$ = 0 V (Note 3)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Negative Power Supply Current | 40 | 55 | 65 | 40 | 55 | 65 | 40 | 55 | 65 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 4) | 1460 | 1510 | 1560 | 1490 | 1540 | 1590 | 1515 | 1565 | 1615 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 4) | | | | | | | | | | mV |
| | ($OLS = V_{CC}$) | 555 | 705 | 855 | 595 | 745 | 895 | 625 | 775 | 925 | |
| | ($OLS = V_{CC}$ − 0.4 V) | 1235 | 1295 | 1355 | 1270 | 1330 | 1390 | 1295 | 1355 | 1415 | |
| | ($OLS = V_{CC}$ − 0.8 V, OLS = FLOAT) | 775 | 895 | 1015 | 810 | 930 | 1050 | 840 | 960 | 1080 | |
| | ($OLS = V_{CC}$ − 1.2 V) | 1455 | 1505 | 1555 | 1490 | 1540 | 1590 | 1510 | 1560 | 1610 | |
| | ($OLS = V_{EE}$) | 1005 | 1095 | 1185 | 1040 | 1130 | 1220 | 1065 | 1155 | 1245 | |
| $V_{OUTPP}$ | Output Voltage Amplitude | | | | | | | | | | mV |
| | ($OLS = V_{CC}$) | 700 | 800 | | 680 | 795 | | 680 | 790 | | |
| | ($OLS = V_{CC}$ − 0.4 V) | 125 | 215 | | 120 | 210 | | 120 | 210 | | |
| | ($OLS = V_{CC}$ − 0.8 V, OLS = FLOAT) | 525 | 615 | | 520 | 610 | | 515 | 605 | | |
| | ($OLS = V_{CC}$ − 1.2 V) | 0 | 5 | | 0 | 0 | | 0 | 5 | | |
| | ($OLS = V_{EE}$) | 325 | 415 | | 320 | 410 | | 320 | 410 | | |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Note 6) D0, $\overline{D0}$, D1, $\overline{D1}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{EE}$ + 1275 | $V_{CC}$− 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 7) D0, $\overline{D0}$, D1, $\overline{D1}$ | $V_{EE}$ | $V_{CC}$− 1400* | $V_{IH}$− 150 | $V_{EE}$ | $V_{CC}$− 1400* | $V_{IH}$− 150 | $V_{EE}$ | $V_{CC}$− 1400* | $V_{IH}$− 150 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@$V_{IH}$) | | 35 | 100 | | 35 | 100 | | 35 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@$V_{IL}$) | | 20 | 100 | | 20 | 100 | | 20 | 100 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

3. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.125 V to −0.965 V.
4. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
5. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
6. $V_{IH}$ cannot exceed $V_{CC}$.
7. $V_{IL}$ always ≥ $V_{EE}$.

**Table 8. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT** $V_{CC}$ = 3.3 V; $V_{EE}$ = 0 V (Note 8)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Negative Power Supply Current | 40 | 55 | 65 | 40 | 55 | 65 | 40 | 55 | 65 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 9) | 2260 | 2310 | 2360 | 2290 | 2340 | 2390 | 2315 | 2365 | 2415 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 9) | | | | | | | | | | mV |
| | (OLS = $V_{CC}$) | 1320 | 1470 | 1620 | 1360 | 1510 | 1660 | 1390 | 1540 | 1690 | |
| | (OLS = $V_{CC}$ − 0.4 V) | 2030 | 2090 | 2150 | 2065 | 2125 | 2185 | 2090 | 2150 | 2210 | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS = FLOAT) | 1550 | 1670 | 1790 | 1585 | 1705 | 1825 | 1615 | 1735 | 1855 | |
| | (OLS = $V_{CC}$ − 1.2 V) | 2260 | 2310 | 2360 | 2290 | 2340 | 2390 | 2315 | 2365 | 2415 | |
| | **(OLS = $V_{EE}$) | 1785 | 1875 | 1965 | 1820 | 1910 | 2000 | 1850 | 1940 | 2030 | |
| $V_{OUTPP}$ | Output Amplitude Voltage | | | | | | | | | | mV |
| | (OLS = $V_{CC}$) | 715 | 815 | | 705 | 805 | | 690 | 800 | | |
| | (OLS = $V_{CC}$ − 0.4 V) | 130 | 220 | | 125 | 215 | | 125 | 215 | | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS = FLOAT) | 550 | 640 | | 545 | 635 | | 540 | 630 | | |
| | (OLS = $V_{CC}$ − 1.2 V) | 0 | 0 | | 0 | 0 | | 0 | 0 | | |
| | **(OLS = $V_{EE}$) | 345 | 435 | | 340 | 430 | | 335 | 425 | | |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Note 11) D0, $\overline{D0}$, D1, $\overline{D1}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 12) D0, $\overline{D0}$, D1, $\overline{D1}$ | $V_{IH}$− 2600 | $V_{CC}$− 1400* | $V_{IH}$− 150 | $V_{IH}$− 2600 | $V_{CC}$− 1400* | $V_{IH}$− 150 | $V_{IH}$− 2600 | $V_{CC}$− 1400* | $V_{IH}$− 150 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@$V_{IH}$) | | 35 | 100 | | 35 | 100 | | 35 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@$V_{IL}$) | | 20 | 100 | | 20 | 100 | | 20 | 100 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and $V_{CC}$ − $V_{EE}$ > 3.0 V, a 2 kΩ resistor should be connected from OLS to $V_{EE}$.

8. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.925 V to −0.165 V.
9. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
10. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
11. $V_{IH}$ cannot exceed $V_{CC}$.
12. $V_{IL}$ always ≥ $V_{EE}$.

**Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT** $V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −2.375 V (Note 13)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Negative Power Supply Current | 40 | 55 | 65 | 40 | 55 | 65 | 40 | 55 | 65 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 14) | −1040 | −990 | −840 | −1010 | −960 | −910 | −985 | −935 | −885 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 14) | | | | | | | | | | mV |
| | −3.465 V ≤ $V_{EE}$ ≤ −3.0 V | | | | | | | | | | |
| | (OLS = $V_{CC}$) | −1980 | −1830 | −1680 | −1940 | −1790 | −1640 | −1910 | −1760 | −1610 | |
| | (OLS = $V_{CC}$ − 0.4 V) | −1270 | −1210 | −1150 | −1235 | −1175 | −1115 | −1210 | −1150 | −1090 | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS =FLOAT) | −1750 | −1630 | −1510 | −1715 | −1595 | −1475 | −1685 | −1565 | −1445 | |
| | (OLS = $V_{CC}$ − 1.2 V) | −1040 | −990 | −940 | −1010 | −960 | −910 | −985 | −935 | −885 | |
| | **(OLS = $V_{EE}$) | −1515 | −1425 | −1335 | −1480 | −1390 | −1300 | −1450 | −1360 | −1270 | |
| | −3.0 V < $V_{EE}$ ≤ −2.375 V | | | | | | | | | | |
| | (OLS = $V_{CC}$) | −1945 | −1795 | −1645 | −1905 | −1755 | −1605 | −1875 | −1725 | −1575 | |
| | (OLS = $V_{CC}$ − 0.4 V) | −1265 | −1205 | −1145 | −1230 | −1170 | −1110 | −1205 | −1145 | −1085 | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS =FLOAT) | −1725 | −1605 | −1485 | −1690 | −1570 | −1450 | −1660 | −1540 | −1420 | |
| | (OLS = $V_{CC}$ − 1.2 V) | −1045 | −995 | −945 | −1010 | −960 | −910 | −990 | −940 | −890 | |
| | (OLS = $V_{EE}$) | −1495 | −1405 | −1315 | −1460 | −1370 | −1280 | −1435 | −1345 | −1255 | |
| $V_{OUTPP}$ | Output Voltage Amplitude | | | | | | | | | | mV |
| | −3.465 V ≤ $V_{EE}$ ≤ −3.0 V | | | | | | | | | | |
| | (OLS = $V_{CC}$) | 715 | 815 | | 705 | 805 | | 690 | 800 | | |
| | (OLS = $V_{CC}$ − 0.4 V) | 130 | 220 | | 125 | 215 | | 125 | 215 | | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS = FLOAT) | 550 | 640 | | 545 | 635 | | 540 | 630 | | |
| | (OLS = $V_{CC}$ − 1.2 V) | 0 | 0 | | 0 | 0 | | 0 | 0 | | |
| | **(OLS = $V_{EE}$) | 345 | 435 | | 340 | 430 | | 335 | 425 | | |
| | −3.0 V < $V_{EE}$ ≤ −2.375 V | | | | | | | | | | |
| | (OLS = $V_{CC}$) | 700 | 800 | | 690 | 795 | | 680 | 790 | | |
| | (OLS = $V_{CC}$ − 0.4 V) | 125 | 215 | | 120 | 210 | | 120 | 210 | | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS =FLOAT) | 525 | 615 | | 520 | 610 | | 515 | 605 | | |
| | (OLS = $V_{CC}$ − 1.2 V) | 0 | 5 | | 0 | 0 | | 0 | 5 | | |
| | (OLS = $V_{EE}$) | 325 | 415 | | 320 | 410 | | 320 | 410 | | |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) (Note 16) D0, $\overline{D0}$, D1, $\overline{D1}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | $V_{EE}$ + 1275 | $V_{CC}$ − 1000* | $V_{CC}$ | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) (Note 17) D0, $\overline{D0}$, D1, $\overline{D1}$ | $V_{IH}$− 2600 | $V_{CC}$− 1400* | $V_{IH}$− 150 | $V_{IH}$− 2600 | $V_{CC}$− 1400* | $V_{IH}$− 150 | $V_{IH}$− 2600 | $V_{CC}$− 1400* | $V_{IH}$− 150 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 15) | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | V |
| $R_{TIN}$ | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
| $I_{IH}$ | Input HIGH Current (@$V_{IH}$) | | 35 | 100 | | 35 | 100 | | 35 | 100 | μA |
| $I_{IL}$ | Input LOW Current (@$V_{IL}$) | | 20 | 100 | | 20 | 100 | | 20 | 100 | μA |
| $I_{OLS}$ | OLS Input Current (See Figure 9) | | | | | | | | | | μA |
| | (OLS = $V_{CC}$) | | 300 | 900 | | 300 | 900 | | 300 | 900 | |
| | (OLS = $V_{CC}$ − 0.4 V) | | 100 | 300 | | 100 | 300 | | 100 | 300 | |
| | (OLS = $V_{CC}$ − 0.8 V, OLS = FLOAT) | | 5 | 100 | | 5 | 100 | | 5 | 100 | |
| | (OLS = $V_{CC}$ − 1.2 V) | −300 | −100 | | −300 | −100 | | −300 | −100 | | |
| | −3.0 V < $V_{EE}$ ≤ −2.375 V | | | | | | | | | | |
| | (OLS = $V_{EE}$) | −1000 | −400 | | −1000 | −400 | | −1000 | −400 | | |
| | −3.465 V ≤ $V_{EE}$ ≤ −3.0 V | | | | | | | | | | |
| | *(OLS = $V_{EE}$) | −1500 | −600 | | −1500 | −600 | | −1500 | −600 | | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and $V_{CC}$ − $V_{EE}$ > 3.0 V, a 2 kΩ resistor should be connected from OLS to $V_{EE}$.

13. Input and output parameters vary 1:1 with $V_{CC}$.
14. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
15. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
16. $V_{IH}$ cannot exceed $V_{CC}$.
17. $V_{IL}$ always ≥ $V_{EE}$.

**Table 10. AC CHARACTERISTICS** $V_{CC}$ = 0 V; $V_{EE}$ = −3.465 V to −2.375 V or $V_{CC}$ = 2.375 V to 3.465 V; $V_{EE}$ = 0 V (Note 18)

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{OUTPP}$ | Output Voltage Amplitude $f_{in}$ < 5 GHz (Note 18) | 400 | 590 | | 450 | 590 | | 440 | 590 | | mV |
| | $f_{in} \leq$ 7 GHz | 200 | 250 | | 180 | 250 | | 130 | 250 | | |
| $t_{PLH}$ | Propagation Delay to Output Differential | | | | | | | | | | ps |
| | D0, D1 → Q0, Q1 | 170 | 205 | 255 | 170 | 205 | 255 | 170 | 210 | 260 | |
| | SELA, SELB → Q0, Q1 | 190 | 265 | 350 | 190 | 265 | 350 | 190 | 265 | 350 | |
| $t_{PHL}$ | Propagation Delay to Output Differential | | | | | | | | | | ps |
| | D0, D1 → Q0, Q1 | 170 | 205 | 255 | 170 | 205 | 255 | 170 | 210 | 260 | |
| | SELA, SELB → Q0, Q1 | 150 | 215 | 270 | 150 | 215 | 270 | 150 | 215 | 270 | |
| $t_{SKEW}$ | Duty Cycle Skew (Note 19) | | | | | | | | | | ps |
| | Within−Device Skew | | 5.0 | 25 | | 5.0 | 25 | | 5.0 | 25 | |
| | Device−to−Device Skew | | 5.0 | 25 | | 5.0 | 25 | | 5.0 | 25 | |
| | | | 15 | 50 | | 15 | 50 | | 15 | 50 | |
| $t_{JITTER}$ | RMS Random Clock Jitter (Note 20) | | | | | | | | | | ps |
| | $f_{in} \leq$ 7 GHz | | 0.2 | 1.5 | | 0.2 | 1.5 | | 0.2 | 1.5 | |
| | Peak−to−Peak Data Dependent Jitter (Note 21) $f_{in} \leq$ 7 Gb/s | | 12 | 18 | | 12 | 18 | | 12 | 18 | |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 22) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| $t_r$ | Output Rise/Fall Times (Q0, Q1) | | | | | | | | | | ps |
| $t_f$ | (20% − 80%) $t_r$ | 40 | 55 | 70 | 40 | 55 | 70 | 40 | 55 | 70 | |
| | @ 1 GHz $t_f$ | 30 | 45 | 55 | 30 | 45 | 55 | 30 | 45 | 55 | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

18. Measured using a 75 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$ − 2.0 V. OLS = FLOAT. Input edge rates 40 ps (20% − 80%).
19. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.
20. Additive RMS jitter with 50% Duty Cycle clock signal at 7 GHz.
21. Additive Peak−to−Peak data dependent jitter with NRZ PRBS $2^{31-1}$ data at 7 Gb/s.
22. Input Voltage Swing is a single−ended measurement operating in differential mode. $V_{INPP}$ (max) cannot exceed $V_{CC} - V_{EE}$.

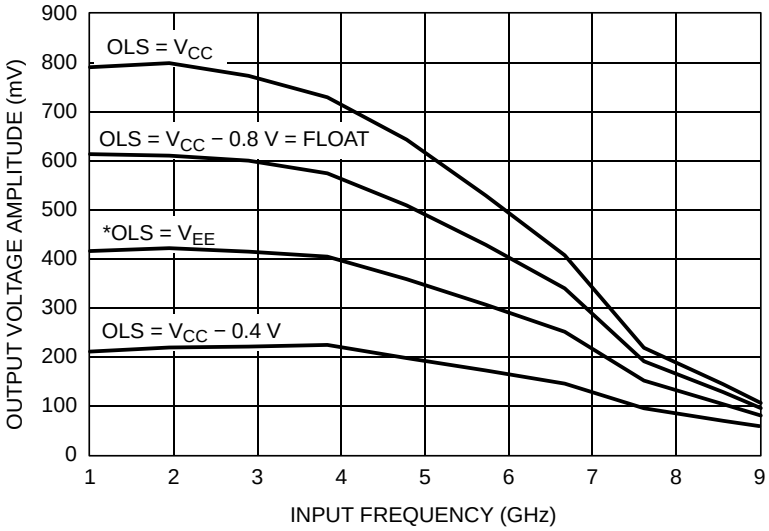



**Figure 3. Output Voltage Amplitude ($V_{OUTPP}$) vs. Input Clock Frequency ($f_{in}$) @ Ambient Temperature (Typical)**

*When an output level of 400 mV is desired and $V_{CC} - V_{EE}$ > 3.0 V, a 2 kΩ resistor should be connected from OLS to $V_{EE}$.

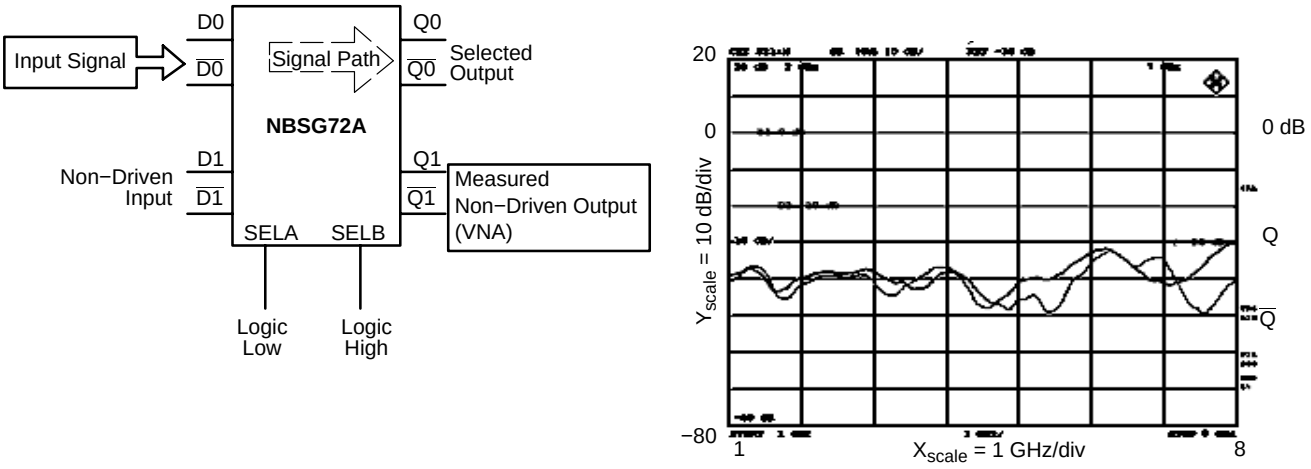



**Figure 4. Channel−to−Channel Crosstalk Isolation at Ambient Temperature (D0 to Q0 Signal Path Selected; SelA = Low, SelB = High)**

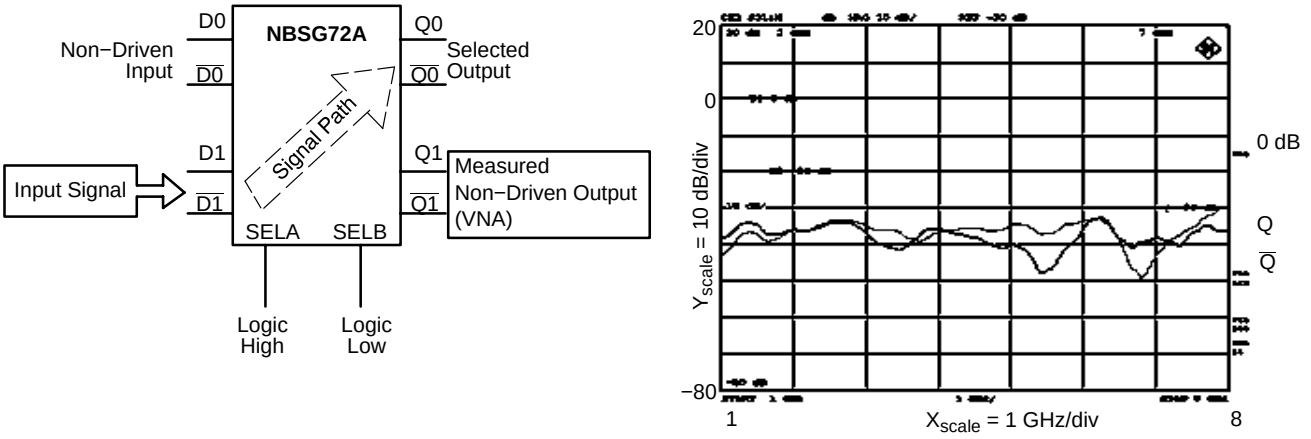



**Figure 5. Channel−to−Channel Crosstalk Isolation at Ambient Temperature (D1 to Q0 Signal Path Selected; SelA = High, SelB = Low)**

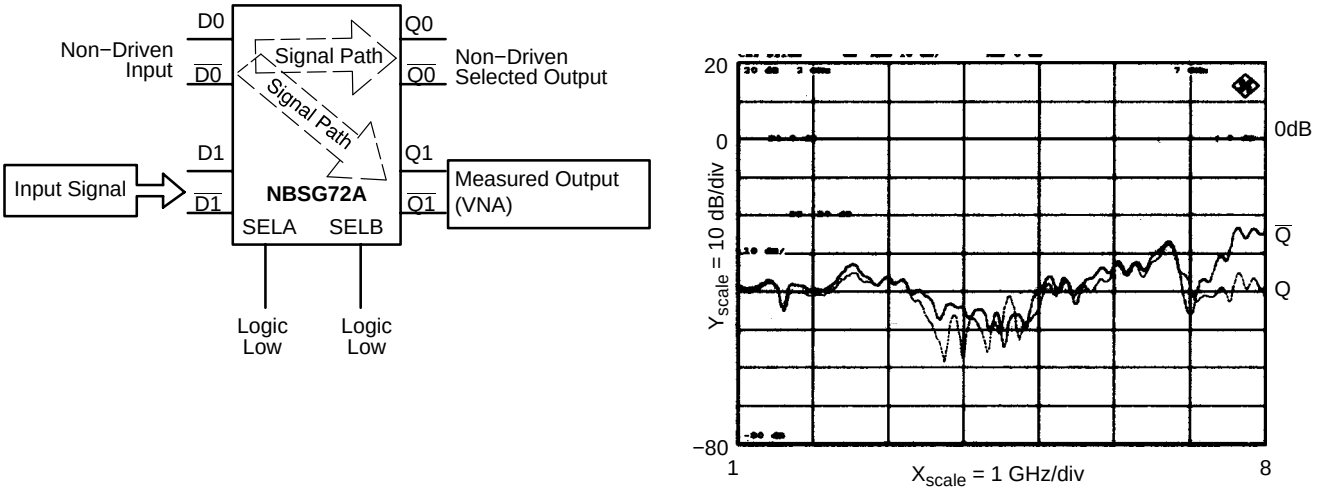



**Figure 6. Channel−to−Channel Crosstalk Isolation at Ambient Temperature (D0 to Q0 and Q1 Signal Path Selected; SelA = Low, SelB = Low)**

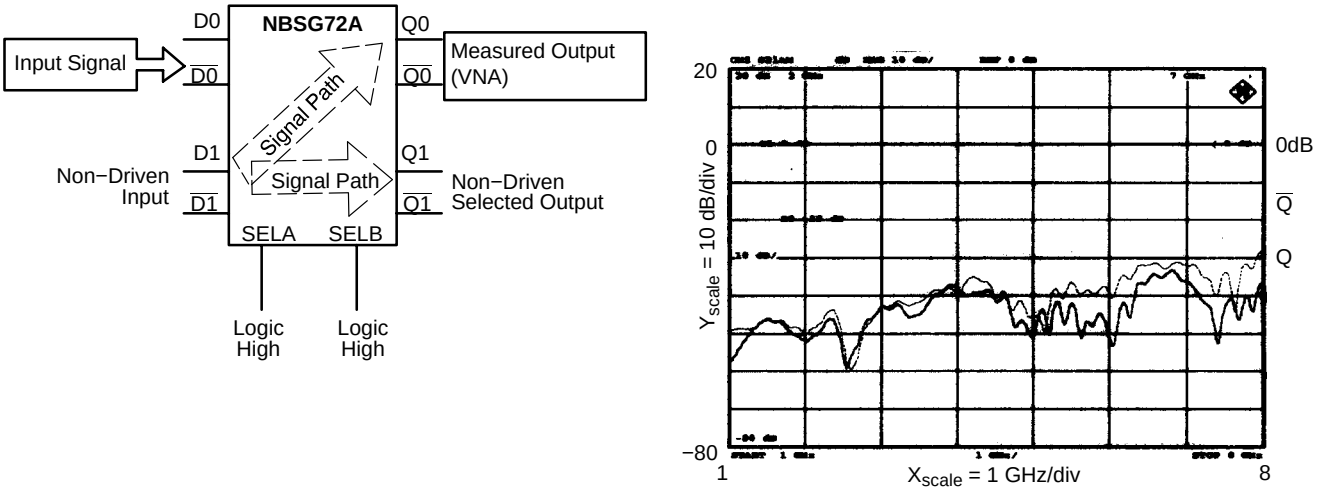
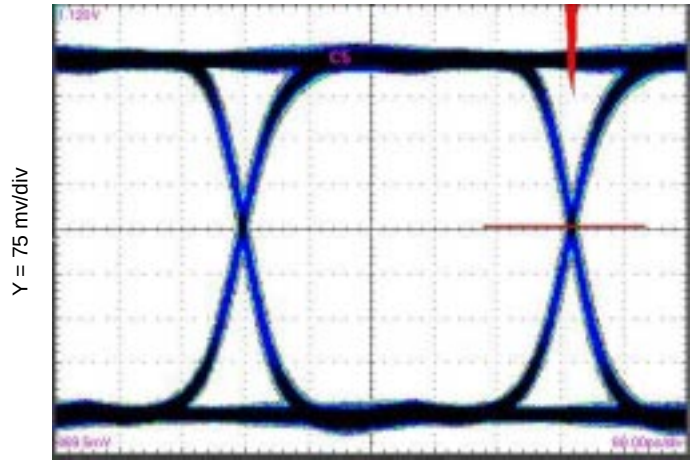
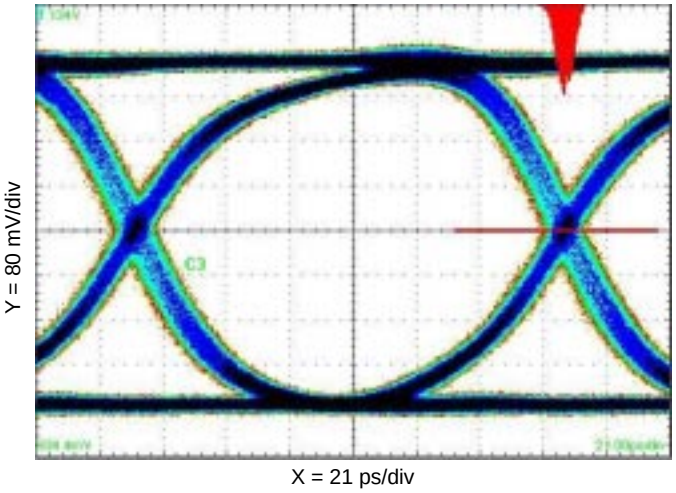



**Figure 7. Channel−to−Channel Crosstalk Isolation at Ambient Temperature (D1 to Q0 and Q1 Signal Path Selected; SelA = High, SelB = High)**




**Total System Jitter = 17.2 ps**
**Input Generator Jitter = 10 ps**
**Device Jitter = 6.8 ps**

**Figure 8. Eye Diagram at 3.2 Gb/s**
**($V_{CC}$ − $V_{EE}$ = 3.3 V, OLS = FLOAT @ 25°C with input pattern of $2^{31-1}$ PRBS, 5000 Waveforms)**




**Total System Jitter = 17.2 ps**
**Input Generator Jitter = 10 ps**
**Device Jitter = 7.2 ps**

**Figure 9. Eye Diagram at 7 GBit/s**
**($V_{CC}$ − $V_{EE}$ = 3.3 V, OLS = FLOAT @ 25°C with input pattern of $2^{31-1}$ PRBS, 5000 Waveforms)**

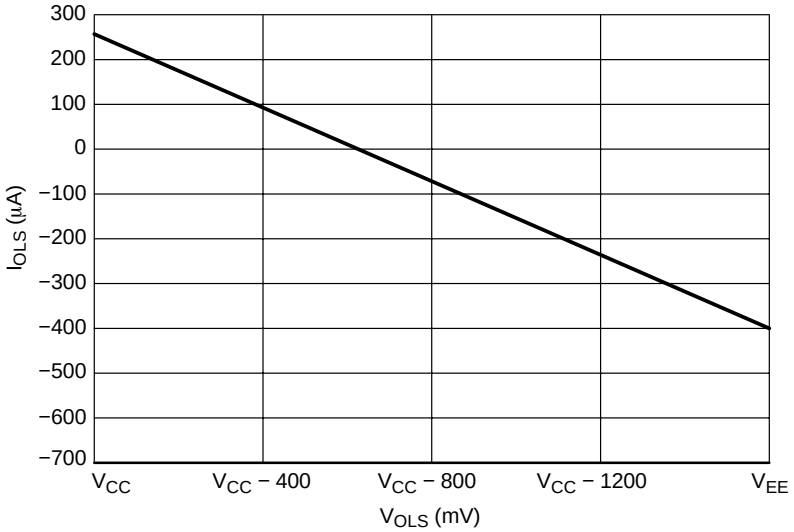



**Figure 10. Typical OLS Input Current vs. OLS Input Voltage**
**($V_{CC}$ − $V_{EE}$ = 3.3 V @ 25°C)**

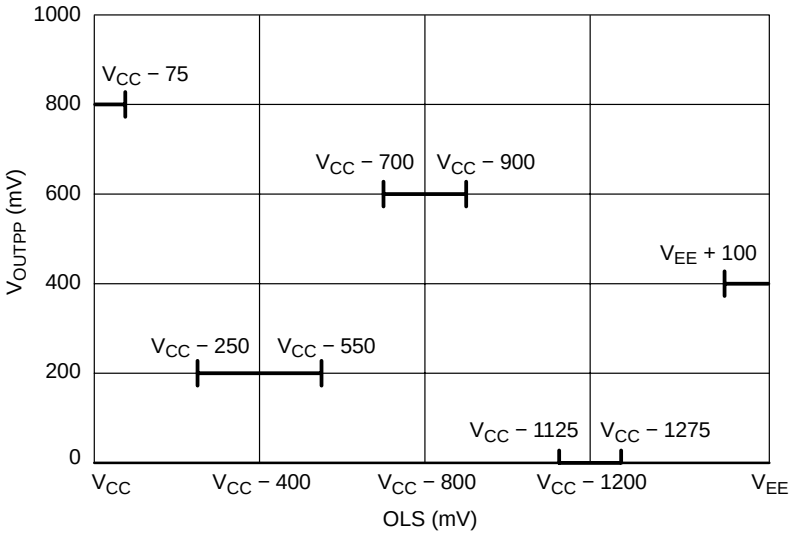



**Figure 11. OLS Operating Area**

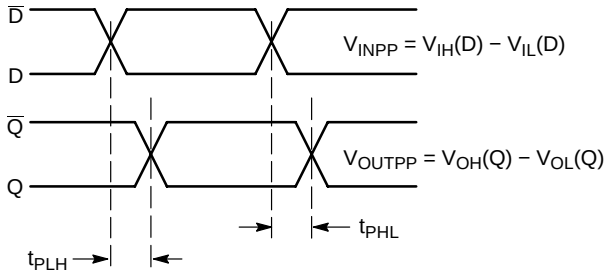



**Figure 12. AC Reference Measurement**

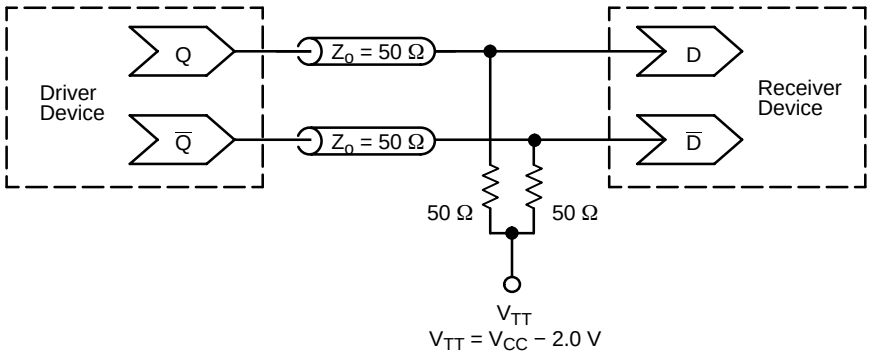



**Figure 13. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NBSG72AMN | QFN−16 | 123 Units / Rail |
| NBSG72AMNG | QFN−16<br>(Pb−Free) | 123 Units / Rail |
| NBSG72AMNR2 | QFN−16 | 3000 / Tape & Reel |

| Board | Description |
|---|---|
| NBSG72AMNEVB | NBSG72AMN Evaluation Board |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** − ECL Clock Distribution Techniques

**AN1406/D** − Designing with PECL (ECL at +5.0 V)

**AN1503/D** − ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** − Metastability and the ECLinPS Family

**AN1568/D** − Interfacing Between LVDS and ECL

**AN1642/D** − The ECL Translator Guide

**AND8001/D** − Odd Number Counters Design

**AND8002/D** − Marking and Date Codes

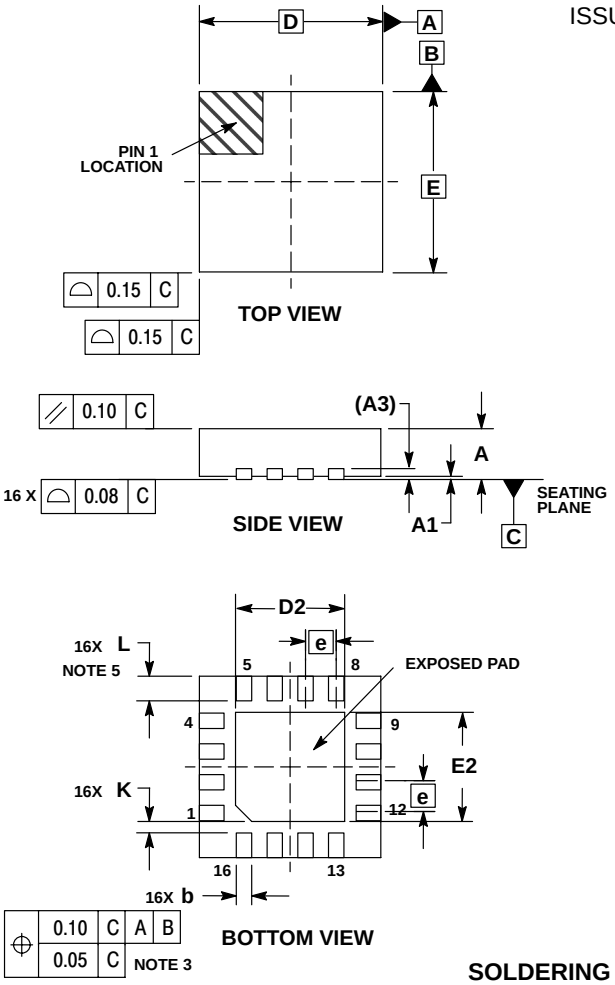
**AND8020/D** − Termination of ECL Logic Devices

**AND8066/D** − Interfacing with ECLinPS

**AND8090/D** − AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

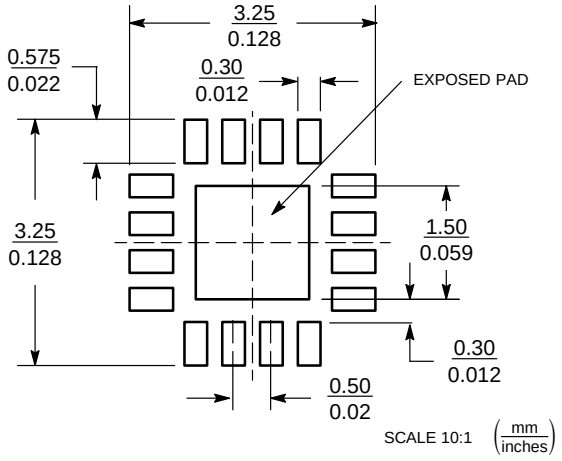
**16 PIN QFN**
**MN SUFFIX**
CASE 485G−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. $L_{max}$ CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 1.65 | 1.85 |
| E | 3.00 BSC | |
| E2 | 1.65 | 1.85 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |

**SOLDERING FOOTPRINT***




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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