

NLAS4783

Triple SPDT 1.0 Ω R_{ON} Switch

The NLAS4783 is a triple independent ultra-low R_{ON} SPDT analog switch with ENABLE. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS4783 can handle a balanced microphone/speaker/ring-tone generator in a monophone mode. The device contains a break-before-make feature.

Features

- Single Supply Operation
1.65 to 3.6 V V_{CC}
- Tiny 3 x 3 mm 16-Pin QFN Package
Meets JEDEC MO-220 Specifications
- Low Static Power
- OVT on Logic Address and Enable Inputs
- This is a Pb-Free Device*

Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Three Unbalanced (Single-Ended) Switches
- Stereo Balanced (Push-Pull) Switching

Important Information

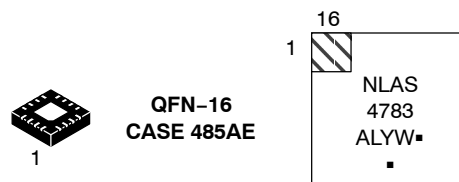
- ESD Protection:
Human Body Model (HBM) > 8000 V
Machine Model (MM) > 400 V
- Ringtone-Chip/Amplifier Switching
- Continuous Current Rating Through each Switch ± 300 mA
- Conforms to: JEDEC MO-220, Issue H, Variation VEED-6
- Pin-for-Pin Compatible with MAX4783



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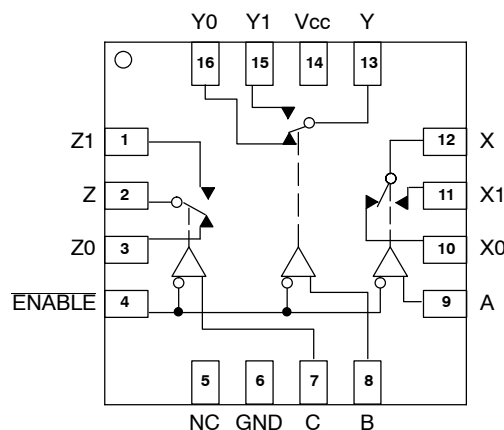
<http://onsemi.com>

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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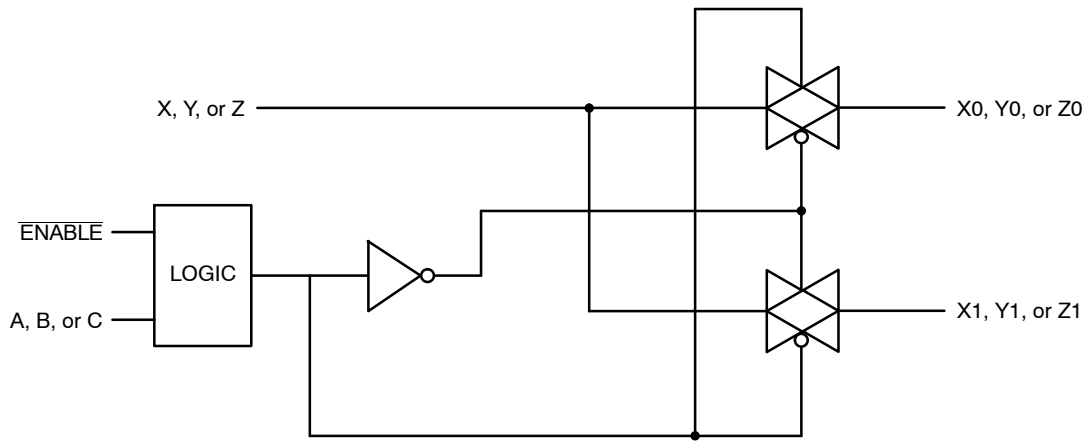


Figure 1. Input Equivalent Circuit

PIN FUNCTION DESCRIPTION

| QFN PIN # | Symbol | Description |
|-----------|-----------------|---|
| 15 | Y1 | Analog Switch Y Normally Open Input |
| 16 | Y0 | Analog Switch Y Normally Closed Input |
| 1 | Z1 | Analog Switch Z Normally Open Input |
| 2 | Z | Analog Switch Z Output |
| 3 | Z0 | Analog Switch Z Normally Closed Input |
| 4 | ENABLE | Digital Enable Input. Normally connect to GND. Drive to logic high to set all switches off. |
| 5 | NC | No Connection. Not internally connected. |
| 6 | GND | Ground |
| 7 | C | Digital Address C Input |
| 8 | B | Digital Address B Input |
| 9 | A | Digital Address A Input |
| 10 | X0 | Analog Switch X Normally Closed Input |
| 11 | X1 | Analog Switch X Normally Open Input |
| 12 | X | Analog Switch X Output |
| 13 | Y | Analog Switch Y Output |
| 14 | V _{CC} | Positive Analog and Digital Supply Voltage Input |

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TRUTH TABLE/SWITCH PROGRAMMING

| Enable Input | Select Input | | | |
|--------------|--------------|---|---|----------------------|
| | C | B | A | |
| H | X | X | X | All Switches Open |
| L | L | L | L | X-X0 Y-Y0 Z-Z0 |
| L | L | L | H | X-X1 Y-Y0 Z-Z0 |
| L | L | H | L | X-X0 Y-Y1 Z-Z0 |
| L | L | H | H | X-X1 Y-Y1 Z-Z0 |
| L | H | L | L | X-X0 Y-Y0 Z-Z1 |
| L | H | L | H | X-X1 Y-Y0 Z-Z1 |
| L | H | H | L | X-X0 Y-Y1 Z-Z1 |
| L | H | H | H | X-X1 Y-Y1 Z-Z1 |

1. Input and output pins are identical and interchangeable. Both pins can be considered input or output. Bidirectional signal pass.

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DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Limit | | Unit |
|------------------|---|---|-----------------|------------------|--------|------|
| | | | | -40°C to 25°C | < 85°C | |
| V _{IH} | Minimum High-Level Input Voltage, Select Inputs | | 1.65 | 1.0 | 1.0 | V |
| | | | 2.7 | 1.4 | 1.4 | |
| | | | 3.6 | 1.8 | 1.8 | |
| V _{IL} | Maximum Low-Level Input Voltage, Select Inputs | | 1.65 | 0.4 | 0.4 | V |
| | | | 2.7 | 0.5 | 0.5 | |
| | | | 3.6 | 0.6 | 0.6 | |
| I _{IN} | Maximum Input Leakage Current, Select Inputs | V _{IN} = 3.6 V or GND | 3.6 | ± 0.1 | ± 1.0 | μA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = 3.6 V or GND | 0 | ± 0.5 | ± 2.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (Note 3) | Select and V _{IS} = V _{CC} or GND | 1.65 to 3.6 | ± 1.0 | ± 2.0 | μA |

DC ELECTRICAL CHARACTERISTICS – Analog Section

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Maximum Limit | | | | Unit |
|--|--|--|-----------------|--------------------------|-----|--------|-----|------|
| | | | | -40°C to 25°C | | < 85°C | | |
| | | | | Min | Max | Min | Max | |
| R _{ON} | NC/NO On-Resistance (Note 3) | V _{IN} ≤ V _{IL} or V _{IN} ≥ V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 100 mA | 2.7 – 3.6 | | 1.0 | | 1.2 | Ω |
| R _{FLAT} | NC/NO On-Resistance Flatness (Notes 3, 5) | I _{COM} = 100 mA V _{IS} = 0 to V _{CC} | 2.7 – 3.6 | | 0.2 | | 0.2 | Ω |
| ΔR _{ON} | On-Resistance Match Between Channels (Notes 3 and 4) | V _{IS} = 1.3 V; I _{COM} = 100 mA | 2.7 – 3.6 | | 0.4 | | 0.6 | Ω |
| I _{NC(OFF)} I _{NO(OFF)} | NC or NO Off Leakage Current (Note 3) | V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 0.3 V V _{COM} = 3.3 V | 3.6 | -5.0 | 5.0 | -10 | 10 | nA |
| I _{COM(ON)} | COM ON Leakage Current (Note 3) | V _{IN} = V _{IL} or V _{IH} V _{NO} 0.3 V or 3.3 V with V _{NC} floating or V _{NC} 0.3 V or 3.3 V with V _{NO} floating V _{COM} = 0.3 V or 3.3 V | 3.6 | -10 | 10 | -100 | 100 | nA |

3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

4. ΔR_{ON} = R_{ON(MAX)} – R_{ON(MIN)} between NC1 and NC2 or between NO1 and NO2.

5. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | V_{CC} (V) | V_{IS} (V) | Guaranteed Maximum Limit | | | | | Unit |
|-----------|--------------------------------|--|-----------------|-----------------|--------------------------|------|-----|--------|-----|------|
| | | | | | -40°C to 25°C | | | < 85°C | | |
| | | | | | Min | Typ* | Max | Min | Max | |
| t_{ON} | Turn-On Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 3 and 4) | 2.3 – 3.6 | 1.5 | | | 25 | | 27 | ns |
| t_{OFF} | Turn-Off Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 3 and 4) | 2.3 – 3.6 | 1.5 | | | 15 | | 20 | ns |
| t_{BBM} | Minimum Break-Before-Make Time | $V_{IS} = 3.0$ $R_L = 300 \Omega$, $C_L = 35$ pF (Figure 2) | 3.0 | 1.5 | 2.0 | 8.0 | | | | ns |

| | | Typical @ 25, $V_{CC} = 3.6$ V | | |
|----------|---|--------------------------------|--|----|
| C_{IN} | Control Pin Input Capacitance | 2.5 | | pF |
| C_{SN} | SN Port Capacitance | 75 | | pF |
| C_D | D Port Capacitance When Switch is Enabled | 240 | | pF |

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Condition | V_{CC} (V) | 25°C | Unit |
|-----------|---|---|-----------------|---------|------|
| | | | | Typical | |
| BW | Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response | V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 3.6 | 17 | MHz |
| V_{ONL} | Maximum Feed-through On Loss | $V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 3.6 | -0.10 | dB |
| V_{ISO} | Off-Channel Isolation | $f = 100$ kHz; $V_{IS} = 1$ V RMS; $C_L = 5$ nF V_{IN} centered between V_{CC} and GND (Figure 5) (Note 6) | 1.65 – 3.6 | -62 | dB |
| Q | Charge Injection Select Input to Common I/O | $V_{IN} = V_{CC}$ to GND, $R_{IS} = 0 \Omega$, $C_L = 1$ nF $Q = C_L \times \Delta V_{OUT}$ (Figure 6) | 1.65 – 3.6 | 50 | pC |
| THD | Total Harmonic Distortion THD + Noise | $F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 2$ V RMS | 3.0 | 0.015 | % |
| VCT | Channel-to-Channel Crosstalk | $f = 100$ kHz; $V_{IS} = 1$ V RMS, $C_L = 5$ pF, $R_L = 50 \Omega$ V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 3.6 | -62 | dB |

6. Off-Channel Isolation = $20 \log_{10} (V_{com}/V_{no})$, V_{com} = output, V_{no} = input to off switch.

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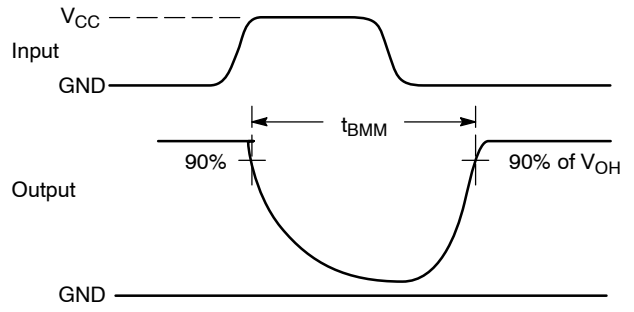
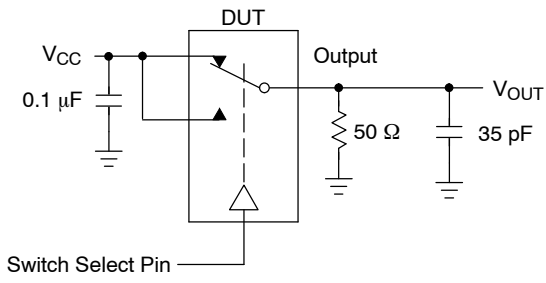


Figure 2. t_{BMM} (Time Break-Before-Make)

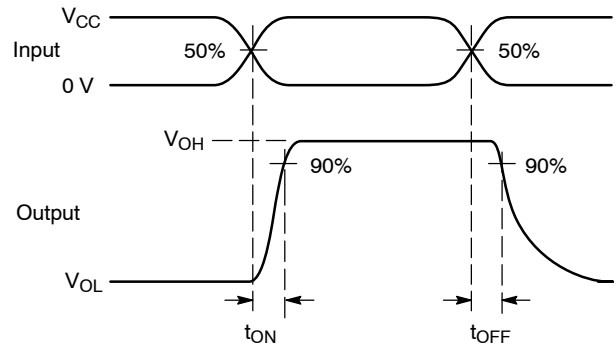
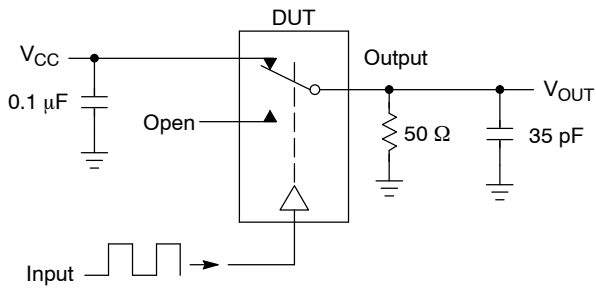


Figure 3. t_{ON}/t_{OFF}

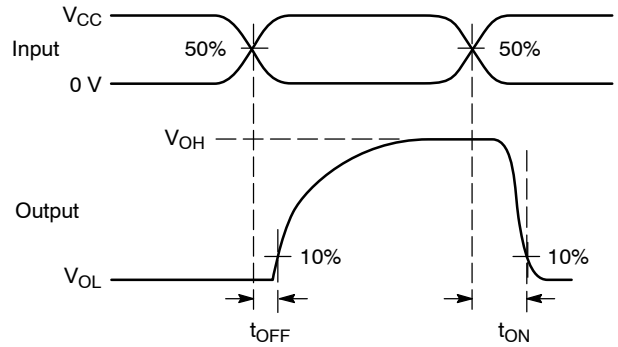
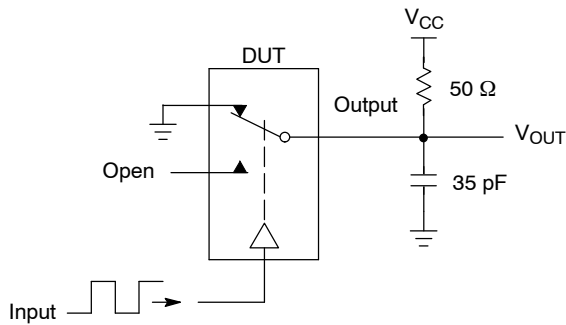
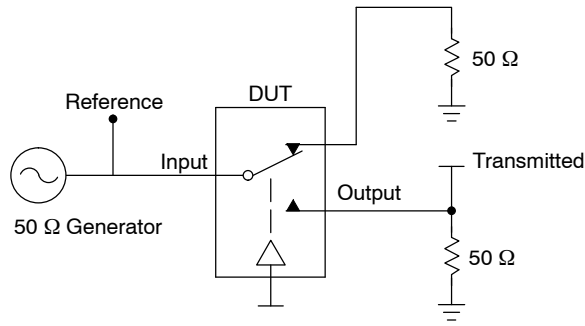


Figure 4. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

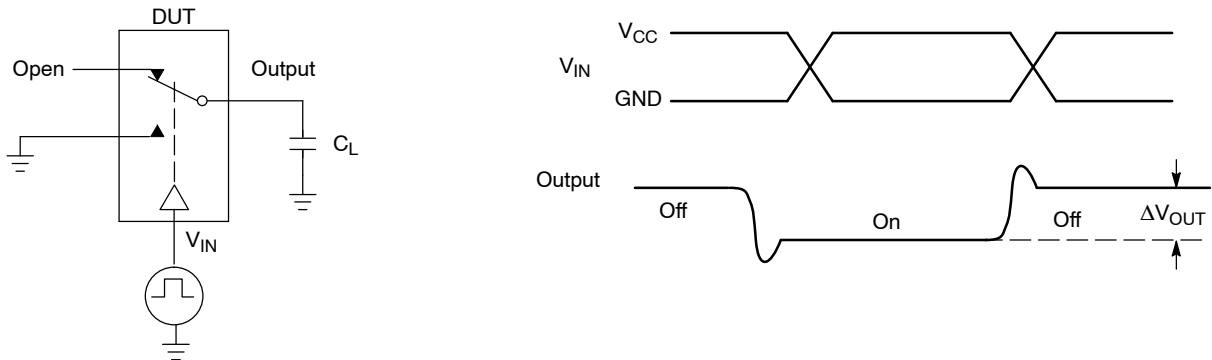


Figure 6. Charge Injection: (Q)

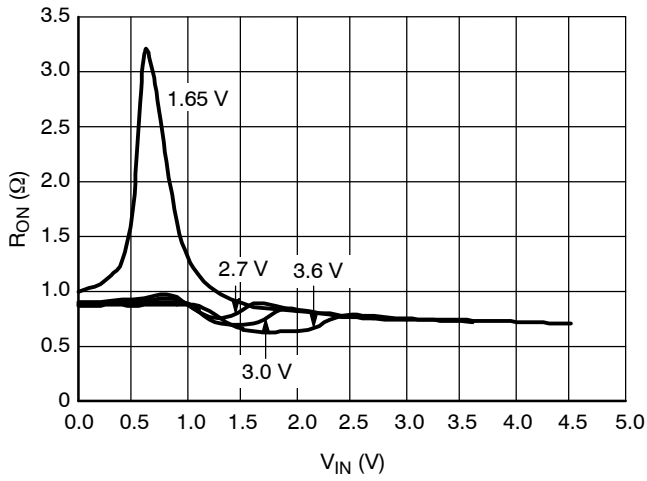


Figure 7. On-Resistance vs. Input Voltage

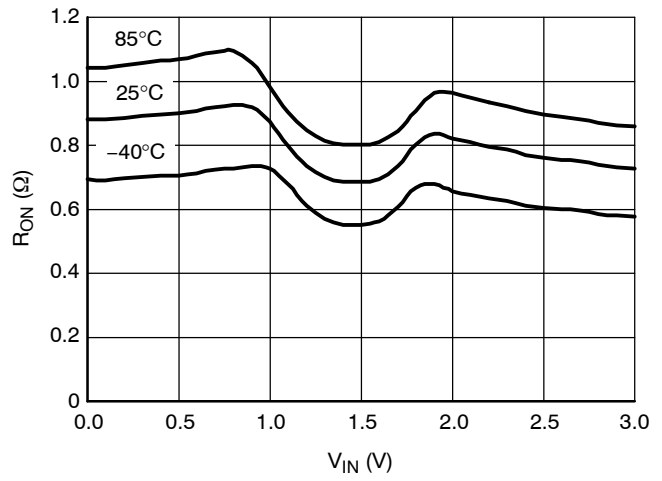


Figure 8. R_{ON} vs. V_{IN} vs. Temperature @ $V_{CC} = 3.0\text{ V}$

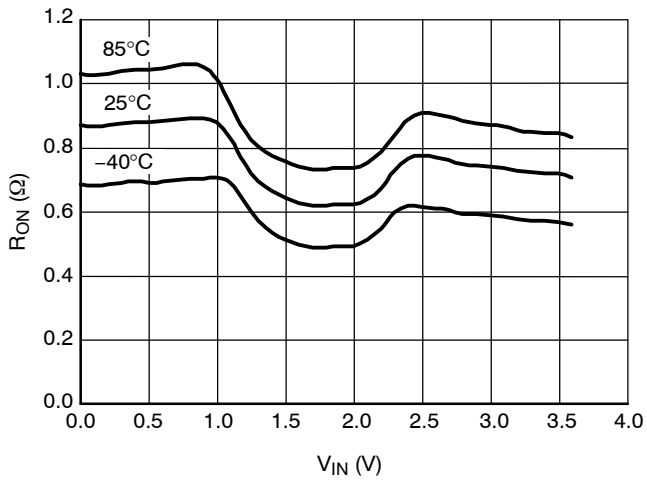


Figure 9. R_{ON} vs. V_{IN} vs. Temperature @ $V_{CC} = 3.6\text{ V}$

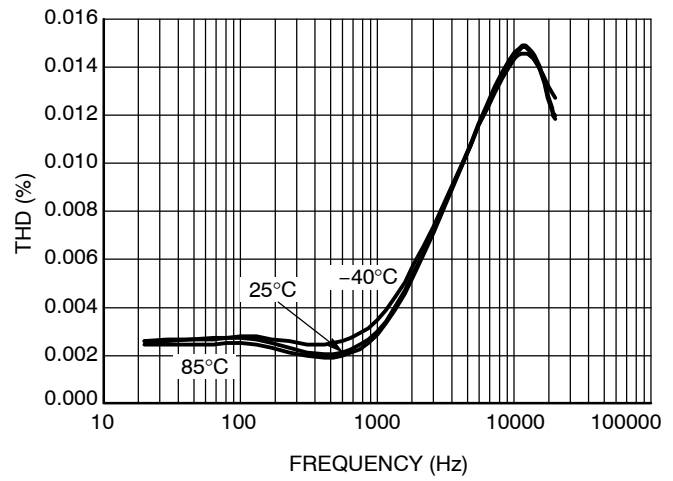


Figure 10. Total Harmonic Distortion vs. Frequency

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ORDERING INFORMATION

| Device Order Number | Device Nomenclature | | | | Package Type | Tape & Reel Size [†] |
|---------------------|---------------------|------------|-----------------|--------------------|------------------|-------------------------------|
| | Circuit Indicator | Technology | Device Function | Tape & Reel Suffix | | |
| NLAS4783MN1R2G | NL | AS | 4783 | R2 | QFN (Pb-Free) | 3000 Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

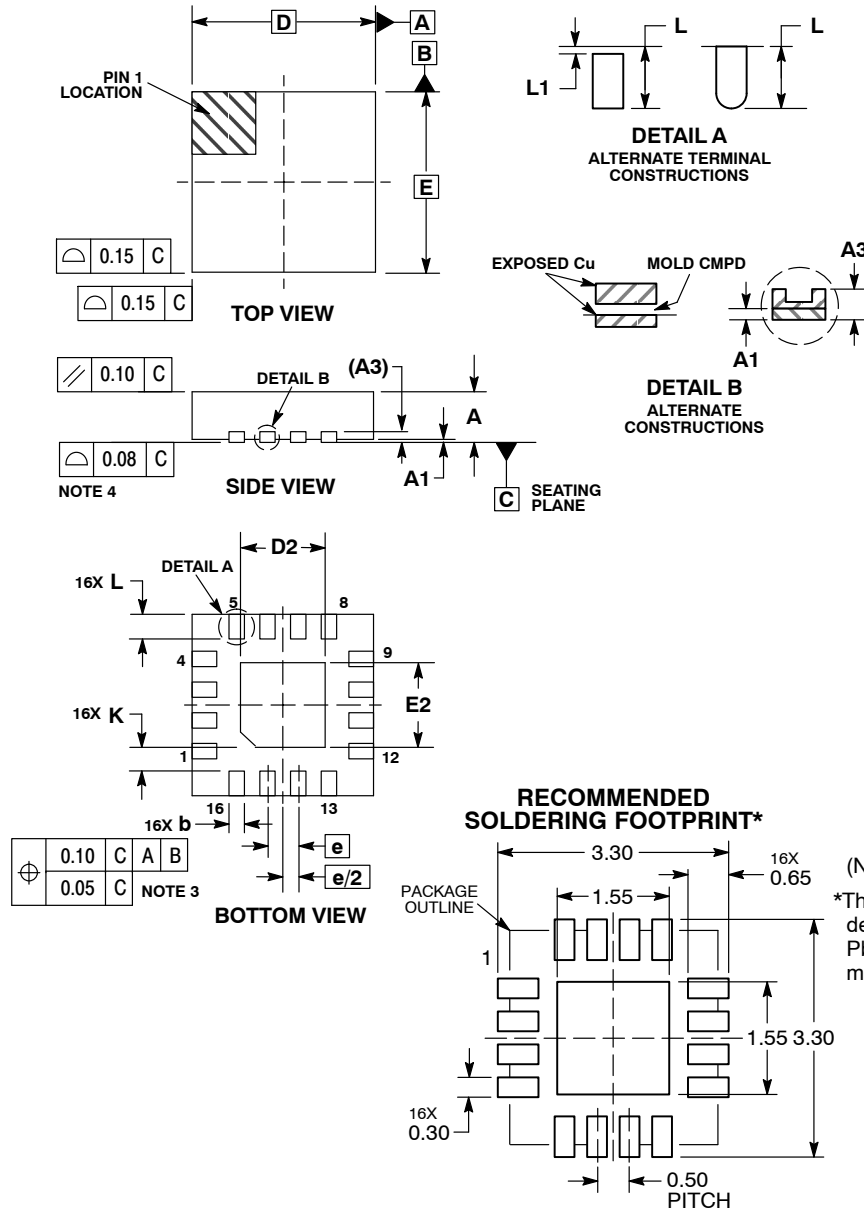
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SCALE 2:1

QFN16 3x3, 0.5P
CASE 485AE
ISSUE C

DATE 24 JUN 2016

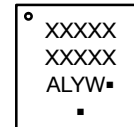


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OUTLINE MEETS JEDEC DIMENSIONS PER MO-220, VARIATION VEED-6.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.25 | 1.55 |
| E | 3.00 | BSC |
| E2 | 1.25 | 1.55 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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