

6.6 mΩ R_{DS(ON)}, 7A, 5.5V V_{IN} Load Switch in 1.2 mm x 2.0 mm VQFN

Features

- Ultra-Low R_{DS(ON)}: 6.6 mΩ Typical
- True 7A Current Capability
- Power Rail Switching from sub-1V to 5.5V
- Bias Voltage from 2.7V to 9V
- ≤1 μA OFF-State Bias Supply Current
- ≤1 μA OFF-State Power Switch Leakage Current
- Adjustable Slew Rate for Inrush Current Limiting by External Capacitor
- Load Discharge
- TTL-Compatible Control Input
- 10-Lead 1.2 mm x 2.0 mm VQFN Package, 0.5 mm Pin Pitch
- -40°C to +125°C Junction Temperature Range

Applications

- Embedded Computing Boards
- Servers
- Data Storage Equipment

General Description

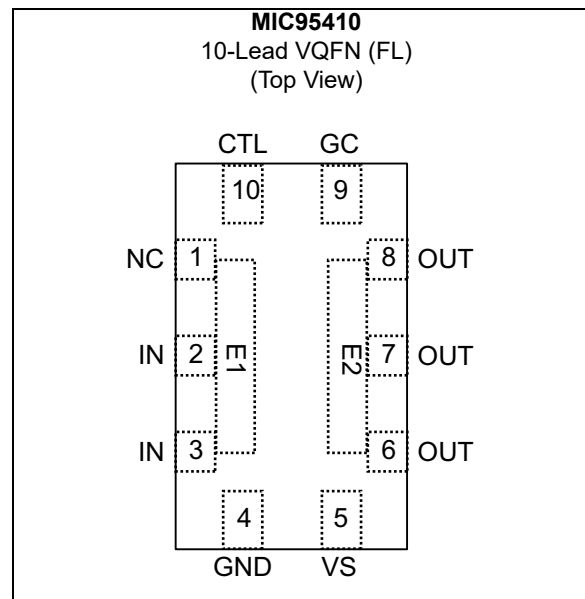
The MIC95410 is a high-side load switch for computing and ultra-dense embedded computing boards where high-current low-voltage rails from sub-1V to 5.5V have to be sectioned. The integrated 6.6 mΩ R_{DS(ON)} N-channel MOSFET ensures low voltage drop and low power dissipation while delivering up to 7A of load current.

The MIC95410 is internally powered by a separated bias voltage from 2.7V to 9V. It includes a TTL-logic level to gate a voltage translator driving a charge pump, and an output discharge function when disabled. The OFF-state current from bias supply (V_S) and the power switch OFF-state leakage current (I_{OFF}) are both below 1 μA.

The MIC95410 provides user-adjustable slew rate controlled turn-on to limit the inrush current to the input supply voltage.

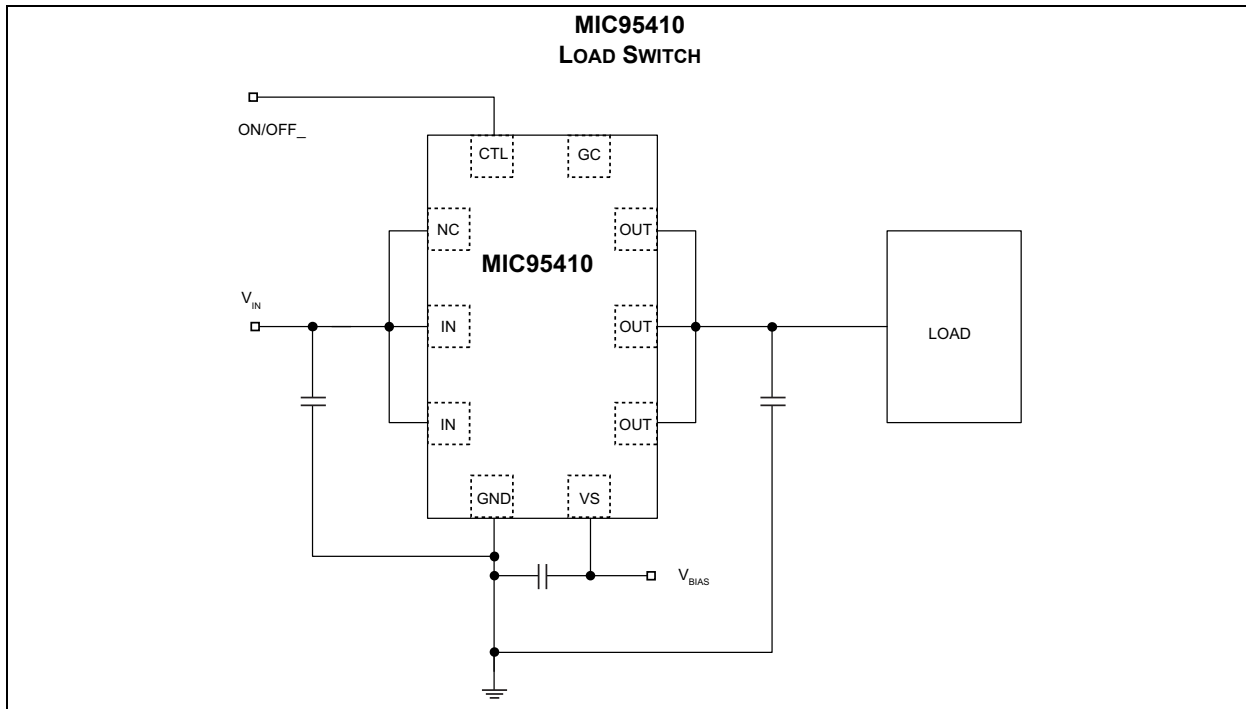
The MIC95410 is available in a thermally efficient, space-saving 10-lead 1.2 mm x 2.0 mm VQFN package with 0.5 mm pin pitch and an operating junction temperature range from -40°C to +125°C.

Package Type

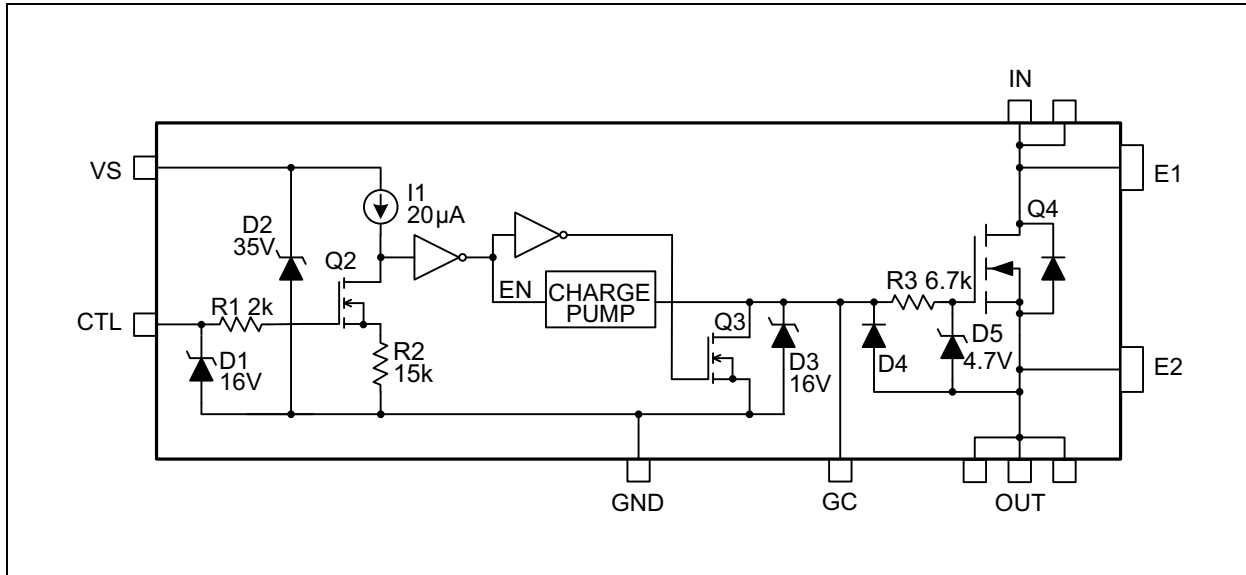


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Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

IN, OUT to GND	-0.3V to +6V
IN to OUT	-0.3V to +6V
IN to GC	+6V
VS to GND	-0.6V to +10V
CTL to GND	+0.6V to V_{VS}
ESD Rating (Note 1)	1.5 kV (HBM)
ESD Rating (Note 1)	150V (MM)

Operating Ratings ††

Input Voltage (V_{IN})	+5.5V
Bias Voltage (V_{VS})	+2.7V to +9V
Gate Connection Voltage (V_{GC})	0V to +11V
ON-State Current (I_{IN})	7A

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 k Ω in series with 100 pF.

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ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{VS} = V_{IN} = V_{CTL} = 5V$, $C_{VS} = 4.7 \mu F$, $C_{IN} = 1 \mu F$, $C_{OUT} = 100 \text{ nF}$, $R = 50 \Omega$ unless otherwise specified. Typical values at $T_A = +25^\circ C$. **Bold** values valid for $-40^\circ C \leq T_A \leq +125^\circ C$, unless noted. [Note 1](#)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Current	I_S	—	0.1	1	μA	$V_{VS} = 3.3V, V_{CTL} = 0V$
		—	—	140		$V_{VS} = 3.3V, V_{CTL} = 3.3V,$ $IN = \text{open}, OUT = \text{open}$
		—	70	90		$V_{VS} = 3.3V, V_{CTL} = 3.3V,$ $IN = \text{open}, OUT = \text{open},$ $T_A = T_J = +25^\circ C$
		—	0.1	1		$V_{VS} = 5V, V_{CTL} = 0V$
		—	—	300		$V_{VS} = 5V, V_{CTL} = 5V,$ $IN = \text{open}, OUT = \text{open}$
		—	150	200		$V_{VS} = 5V, V_{CTL} = 5V,$ $IN = \text{open}, OUT = \text{open},$ $T_A = T_J = +25^\circ C$
Control Input Voltage	V_{CTL}	0	—	0.8	V	$2.7V \leq V_{VS} \leq 9V, \text{logic-0}$
		2.0	—	V_{VS}		$2.7V \leq V_{VS} \leq 5V, \text{logic-1}$
		2.4	—	V_{VS}		$5V < V_{VS} \leq 9V, \text{logic-1}$
Control Input Current	I_{CTL}	—	0.01	1	μA	$2.7V \leq V_{VS} \leq 9V$
Control Input Capacitance	C_{CTL}	—	5	—	pF	—
Switch ON-Resistance	R_{ON}	—	6.6	9.9	m Ω	$V_{VS} = 2.7V, V_{IN} = 1V,$ $I_{IN} = I_{OUT} = 4A$
		—	6.6	9.9		$V_{VS} = 3.3V, V_{IN} = 3.3V,$ $I_{IN} = I_{OUT} = 4A$
		—	6.6	9.9		$V_{VS} = 5V, V_{IN} = 5V,$ $I_{IN} = I_{OUT} = 4A$
Switch Input Leakage Current	I_{OFF}	—	0.02	1	μA	$V_{VS} = 5V, V_{IN} = 5.5V, V_{CTL} = 0V$
Gate Charge Current	I_{GC}	—	27	—	μA	$V_{GC} = 4.0V, R_{LOAD} = \infty$
		—	630	—		$V_{GC} = 0.5V, R_{LOAD} = \infty$
Turn-On Time (Note 2)	t_{ON}	—	1.1	2.0	ms	$C_{GC} = 10 \text{ nF}, V_{IN} = 5V$
		—	0.4	1.0		$C_{GC} = 100 \text{ nF}, V_{IN} = 1V$
Turn-Off Time (Note 3)	t_{OFF}	—	30	60	μs	$C_{GC} = 10 \text{ nF}, V_{IN} = 5V, C_3 = 0 \mu F$
		—	150	300		$C_{GC} = 100 \text{ nF}, V_{IN} = 1V, C_3 = 0 \mu F$
Discharge Resistance	R_D	—	2.3	—	k Ω	$V_{OUT} = 5V, R_{LOAD} = \infty$
		—	2.0	—		$V_{OUT} = 4V, R_{LOAD} = \infty$
		—	1.7	—		$V_{OUT} = 2.5V, R_{LOAD} = \infty$
Discharge Diode Forward Drop ($V_{OUT} - V_{CG}$)	V_D	—	0.5	0.75	V	$V_{CTL} = 0V, I_{OUT} = -10 \mu A$

Note 1: Specification for packaged product only.

2: The turn-on time is defined as the time it takes from asserting CTL to V_{OUT} reaching 90% of V_{IN} (rising).

3: The turn-off time is defined as the time it takes from the falling edge of CTL to V_{OUT} reaching 90% of V_{IN} (falling).

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	-40	—	+125	°C	Note 1
Storage Temperature Range	T_S	-65	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 10 sec.
Package Thermal Resistance						
Thermal Resistance, VQFN 10-Ld	θ_{JA}	—	60	—	°C/W	—

Note 1: Sustained junction temperatures above +125°C can impact the device reliability.

2: Junction-to-Ambient Thermal Resistance θ_{JA} is measured using the Evaluation Board as described in section PCB Layout Recommendations.

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2.0 TYPICAL OPERATING CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

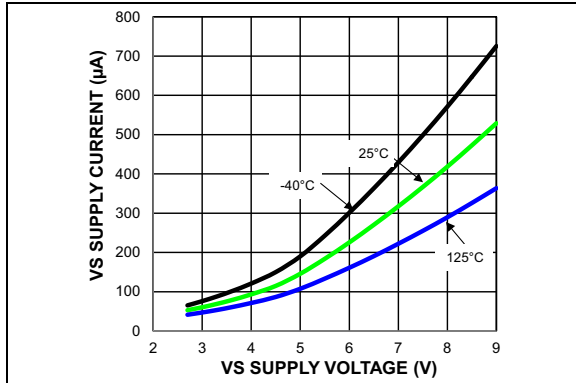


FIGURE 2-1: VS Supply Current vs. VS Supply Voltage.

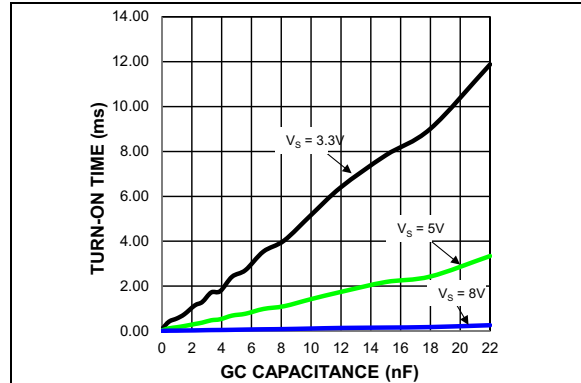


FIGURE 2-4: Turn-On Time vs. GC Capacitance, $V_{IN} = 5V$.

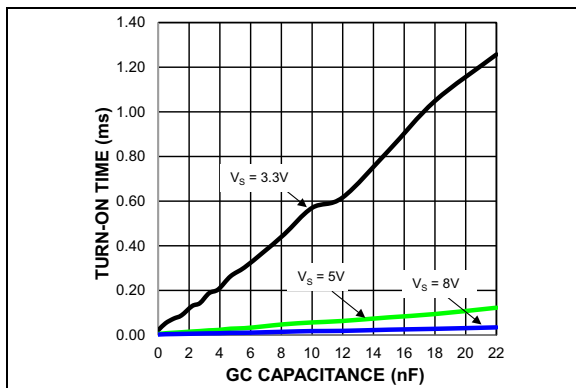


FIGURE 2-2: Turn-On Time vs. GC Capacitance, $V_{IN} = 1.05V$.

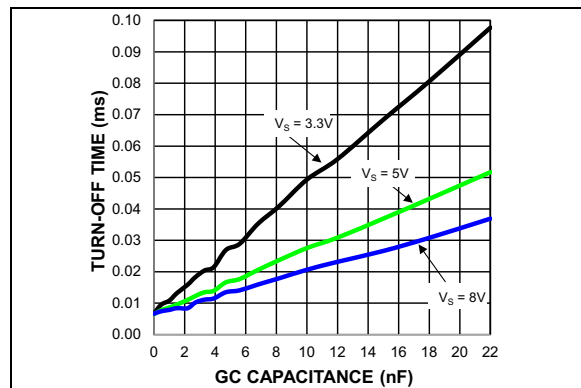


FIGURE 2-5: Turn-Off Time vs. GC Capacitance, $V_{IN} = 1.05V$.

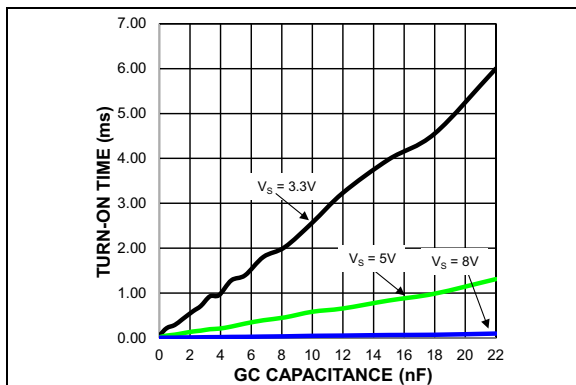


FIGURE 2-3: Turn-On Time vs. GC Capacitance, $V_{IN} = 3.3V$.

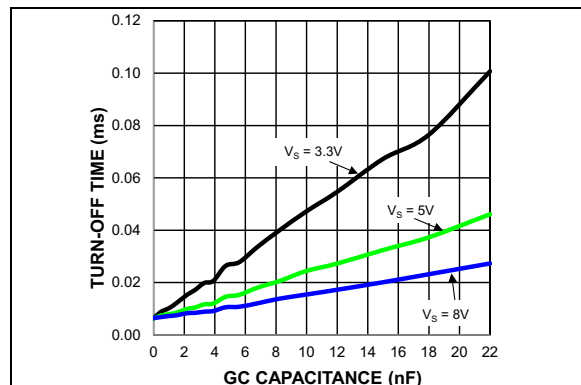


FIGURE 2-6: Turn-Off Time vs. GC Capacitance, $V_{IN} = 3.3V$.

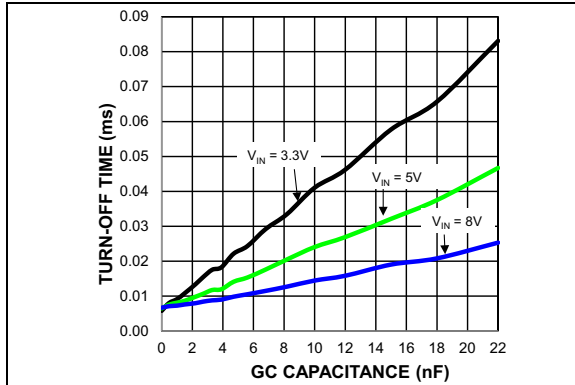


FIGURE 2-7: Turn-Off Time vs. GC Capacitance, $V_{IN} = 5V$.

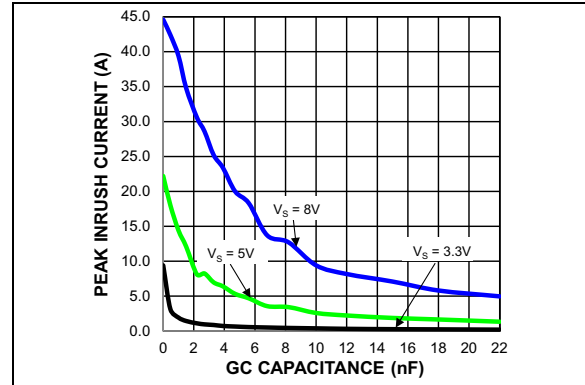


FIGURE 2-10: Initial Peak Inrush Current (Input) vs. GC Capacitance, $V_{IN} = 5V$, $C_{LOAD} = 100 \mu F$.

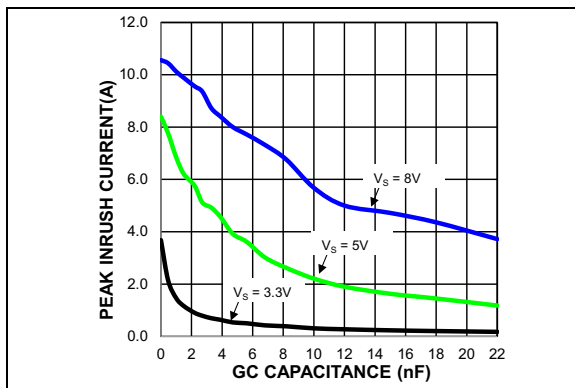


FIGURE 2-8: Initial Peak Inrush Current (Input) vs. GC Capacitance, $V_{IN} = 1.05V$, $C_{LOAD} = 100 \mu F$.

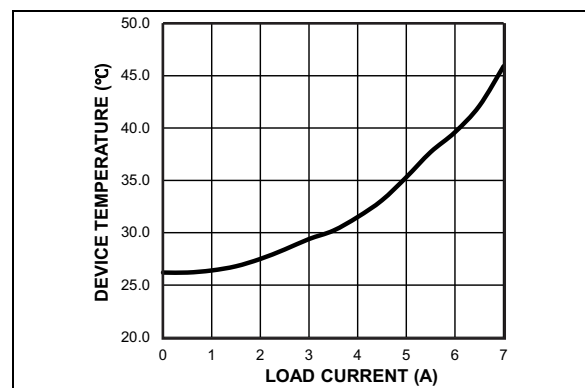


FIGURE 2-11: Device Temperature (Top of Package) vs. Load Current, $V_{IN} = 5V$, $V_{VS} = 5V$.

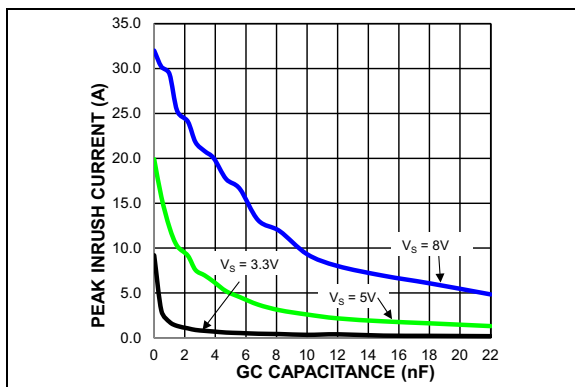


FIGURE 2-9: Initial Peak Inrush Current (Input) vs. GC Capacitance, $V_{IN} = 3.3V$, $C_{LOAD} = 100 \mu F$.

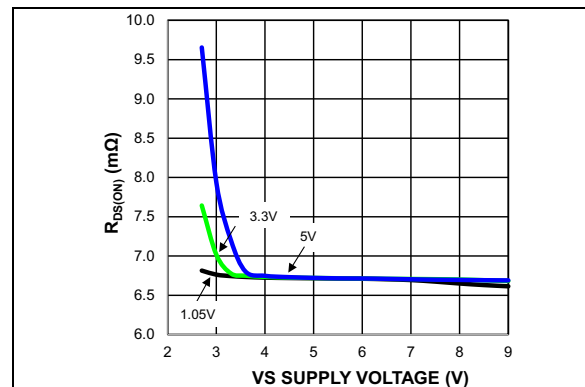


FIGURE 2-12: $R_{DS(ON)}$ vs. Supply Voltage.

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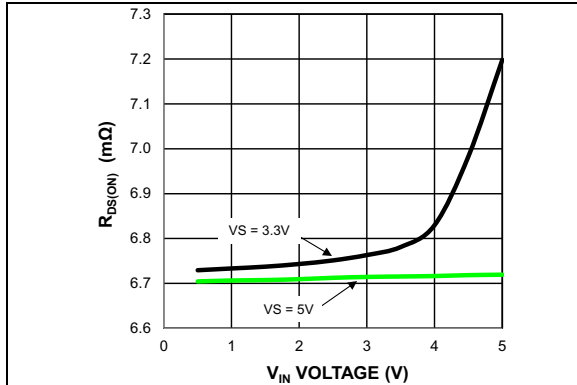


FIGURE 2-13: $R_{DS(ON)}$ vs. V_{IN} Voltage.

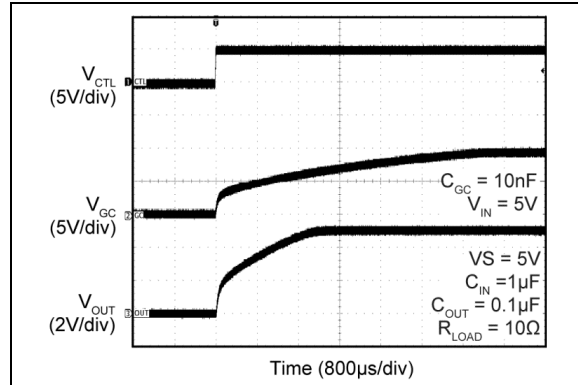


FIGURE 2-16: Turn-On Response.

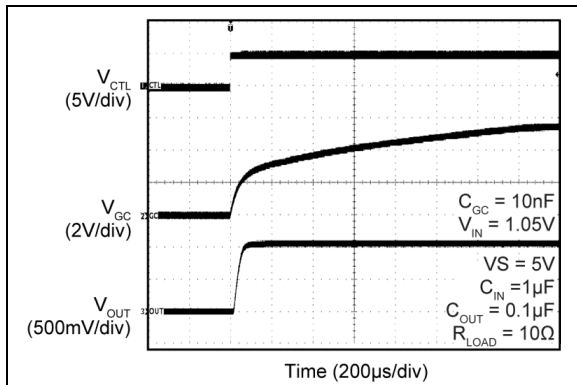


FIGURE 2-14: Turn-On Response.

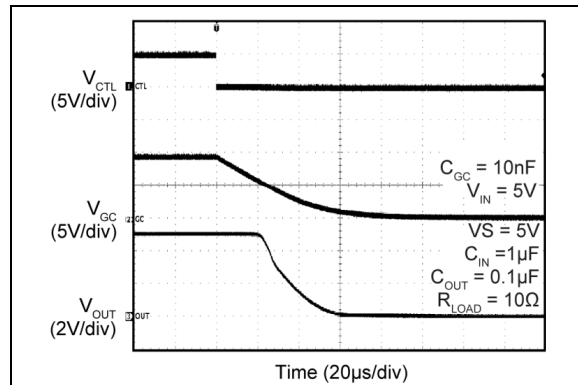


FIGURE 2-17: Turn-Off Response.

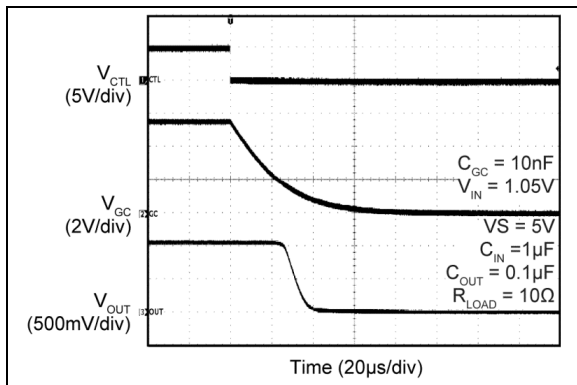


FIGURE 2-15: Turn-Off Response.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	NC	Not internally connected. It is recommended to connect pin 1 to IN such that the width of the input trace can be maximized in the layout.
2, 3, E1	IN	Power switch input (up to 5.5V).
4	GND	Driver ground and discharge return.
5	VS	Bias supply input (2.7V to 9V). Bypass with 4.7 μ F ceramic capacitor to GND.
6, 7, 8, E2	OUT	Power switch output.
9	GC	Gate connection of power FET. Add a ceramic capacitor from GC to ground GND for slew rate control.
10	CTL	Control input. TTL compatible. Logic high enables the power switch. A logic low disables the power switch and discharges OUT.

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4.0 FUNCTIONAL DESCRIPTION

The MIC95410 is a non-inverting device. Applying a logic-high signal to control input (CTL) turns on an internal N-channel MOSFET switch (Q4). The gate control (GC) output can be used to reduce the turn-on speed of the MOSFET by connecting a capacitor from GC to ground.

4.1 Supply

Supply (VS) is rated for +2.7V to +9V. An external 4.7 μ F capacitor (minimum) is recommended.

4.2 ON/OFF Control

Control (CTL) is a TTL-compatible input. CTL must be forced high or low by an external signal. A floating input may cause unpredictable operation.

A high input turns on Q2, which sinks the output of current source I1, and makes the input of the first inverter low. The inverter output becomes high, enabling the charge pump.

4.3 Charge Pump

The charge pump is enabled when CTL is logic high. The charge pump is powered from VS and consists of an oscillator and a 4x voltage multiplier. Output voltage is limited to 16V by an internal Zener diode. The charge pump output current raises the voltage on the GC pin and causes the internal MOSFET Q4 to be turned on. The gate-source voltage of Q4 is internally limited by R3 and D5.

The charge pump oscillator operates from approximately 70 kHz to approximately 100 kHz depending upon the supply voltage and temperature.

4.4 Gate Control

The charge pump output is connected directly to the GC output. The charge pump is active only when CTL is high. When CTL is low, Q3 is turned on by the second inverter and discharges the gate of Q4 to force it off.

If CTL is high, and the voltage applied to VS drops to zero, the gate output will be floating and unpredictable.

4.5 ESD Protection

D1 and D2 clamp positive and negative ESD voltages. R1 isolates the gate of Q2 from sudden changes on the CTL input. Zener D3 also clamps ESD voltages for the GC output. D4 protects the gate of Q4 from ESD on the GC pin.

5.0 APPLICATION INFORMATION

5.1 Turn-On

The MIC95410 is turned on by setting CTL $\geq 2.0V$. The CTL pin enables the MIC95410, which releases the pull-down on GC and starts the charge pump. When the charge pump is turned on, the OUT waveform will exhibit a two-stage rise-time. In the first stage, a higher drive current causes GC to rise rapidly, while in the second phase a lower drive current causes GC to rise more slowly. This is shown in Figure 5-1. With a purely capacitive load C_{OUT} , the current exhibits an initial peak (I_{PEAK}) during the first stage and a limiting, flattening value I_{CHARGE} in the second stage.

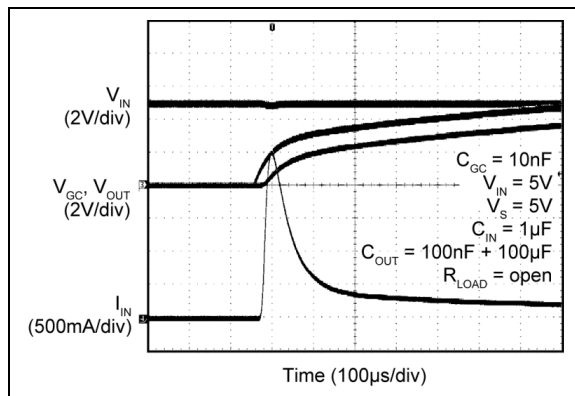


FIGURE 5-1: OUT Voltage and Inrush Current Waveform During Turn-On (IN Current Scale is 500 mA/div).

An analytical prediction of I_{PEAK} is complicated because it involves many factors. For an estimation of I_{PEAK} , and selection of the GC capacitor, the user can refer to the corresponding [Typical Operating Characteristics](#) plots (given for $C_{OUT} = 100 \mu F$), and scale the values in proportion to the actual capacitive load. Note that these plots do not include any additional DC loads because large load capacitances are the most important factor to consider in initial peak inrush current estimation. DC contributions are either negligible at very low output voltage (e.g. resistive load) or typically activated when the OUT voltage has already approached its final value.

The input current during the second (flattening) stage can be estimated as shown in [Equation 5-1](#):

EQUATION 5-1:

$$I_{CHARGE} = \frac{I_{STAGE2} \times C_{OUT}}{C_{GC}}$$

For example, if $C_{GC} = 10 \text{ nF}$, $C_{OUT} = 100 \mu F$ (no additional DC load), $I_{STAGE2} = 27 \mu A$ (see I_{GC} parameter in the [Electrical Characteristics](#) table) then we obtain $I_{CHARGE} = 0.27A$. This calculation is in reasonable agreement with the measurement shown in [Figure 5-1](#).

Note that for very low input voltages, the duration of the turn-on transition is likely to be dominated by the first stage, where the I_{GC} current is much stronger than in the second stage. In this case, an increase of the C_{GC} capacitance could be needed.

Also note that during turn-on the internal power switch can instantaneously dissipate a large amount of power due to the transition through the linear region. Depending upon the instantaneous values of load current and voltage, make sure the turn-on V-I trajectory stays within the Safe Operating Area plot shown in the [Power Switch SOA](#) section.

5.2 Turn-Off

The turn-off of the MIC95410 is started by taking CTL to a logic low where the GC pin is pulled to GND with a resistive MOSFET switch of approximately 2 k Ω (see MOSFET Q3 in the [Functional Block Diagram](#)). Pulling GC to GND will cause the power MOSFET to be turned off (see MOSFET Q4 in the [Functional Block Diagram](#)). Further, the diode D4 between the OUT pin and the GC pin turns on and discharges OUT with a controlled discharge path (D4-Q3).

5.3 Power Dissipation Considerations

The junction temperature (T_J) can be estimated from power dissipation, ambient temperature, and the junction-to-ambient thermal resistance (θ_{JA}).

EQUATION 5-2:

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

For steady-state condition, P_{DISS} is calculated as $I_{IN}^2 \times R_{ON(MAX)}$. θ_{JA} is found in the [Operating Ratings](#) section of the data sheet. This is the value of θ_{JA} measured in still air on the evaluation kit board. Note that the actual θ_{JA} in the final application is strongly dependent on the PCB layout, on the PCB thermal properties, as well as cooling techniques (e.g. forced convection vs. still air). Therefore, the θ_{JA} value given for the evaluation kit board should be used with caution when trying to estimate T_J in the end user application.

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5.4 Power Switch SOA

The safe operating area (SOA) curve shown in [Figure 5-2](#) represents the boundary of maximum safe operating current and voltage for transient operation.

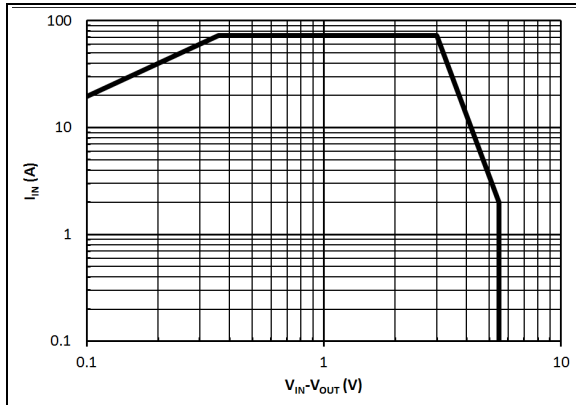


FIGURE 5-2: MIC95410 Power Switch Safe Operating Area.

Ensure that the V-I trajectory stays within recommended SOA boundaries during the turn-on and turn-off transients.

Also note that the SOA plot does not provide safe operating limits for continuous operation and it is only applicable for transient operation. For continuous (DC) operation, the allowable power dissipation limit is dictated by the ambient temperature T_A and the actual θ_{JA} of the device in the end user application as follows:

EQUATION 5-3:

$$P_{DISS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where:

$$T_{J(MAX)} = 125^{\circ}\text{C}.$$

6.0 PCB LAYOUT RECOMMENDATIONS

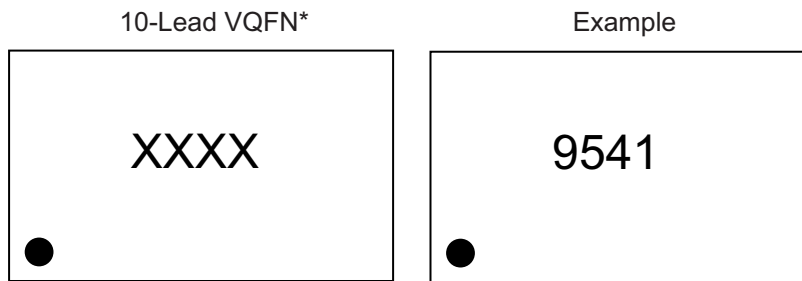
The IN and OUT traces should be made as wide as possible because the main heat-sinking action will be performed by heat removal through the IN/E1 and OUT/E2 connections on the top layer. The traces should widen up as soon as space constraints allow it.

Note that a two-layer routing is adequate for a very compact solution. In case multiple internal planes are used, it is recommended to keep internal planes as solid as possible and to extend them under the MIC95410 and its vicinity (in special the IN and OUT top traces) in order to increase vertical, then lateral, heat transfer.

Another method is to copy the IN and OUT traces on the bottom layer and to stitch them through many thermal vias to the top layers IN and OUT connections, in particular in the immediate vicinity of the MIC95410 IC.

7.0 PACKAGING INFORMATION

7.1 Package Marking Information



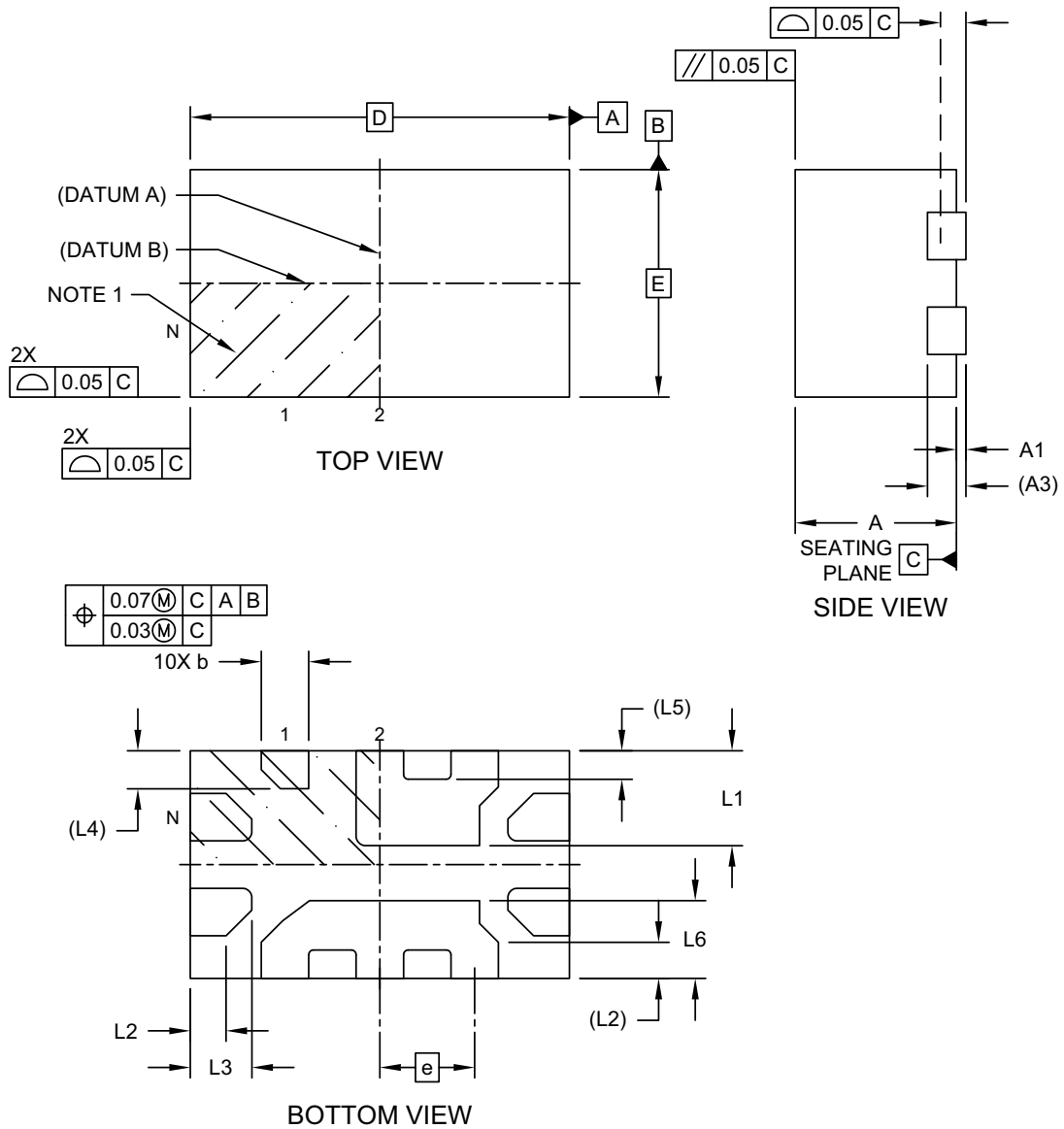
<p>Legend: XX...X Product code or customer-specific information Y Year code (last digit of calendar year) YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code (e3) Pb-free JEDEC® designator for Matte Tin (Sn) * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.</p> <p>•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).</p>
<p>Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.</p> <p>Underbar (_) and/or Overbar (¯) symbol may not be to scale.</p>

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10-Lead VQFN Package Outline and Recommended Land Pattern

10-Lead Very Thin Plastic Quad Flat, No Lead Package (NDA) - 1.2x2.0x0.9 mm Body [VQFN]; Micrel Legacy Package FQFN1220-10LD-PL-1

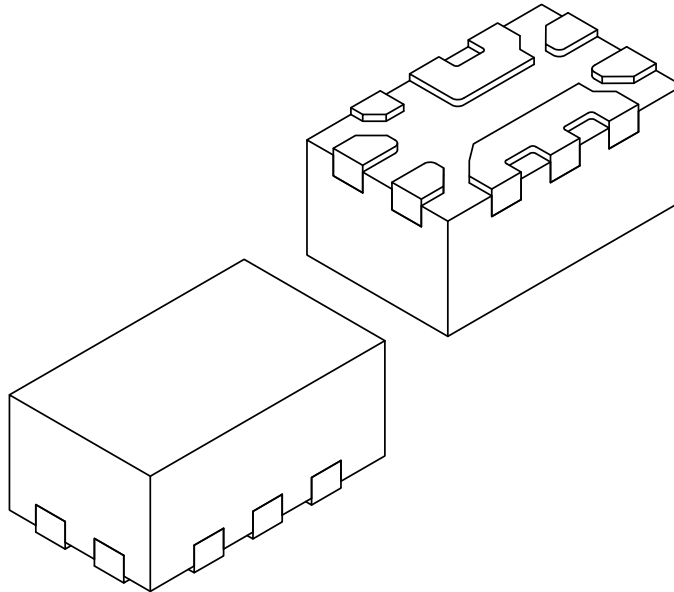
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1029 Rev A Sheet 1 of 2

10-Lead Very Thin Plastic Quad Flat, No Lead Package (NDA) - 1.2x2.0x0.9 mm Body [VQFN]; Micrel Legacy Package FQFN1220-10LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	1.20 BSC		
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L1	0.45	0.50	0.55
Terminal Length	L2	0.19 REF		
Terminal Length	L3	0.275	0.325	0.375
Terminal Length	L4	0.20 REF		
Terminal Length	L5	0.15 REF		
Terminal Length	L6	0.36	0.41	0.46

Notes:

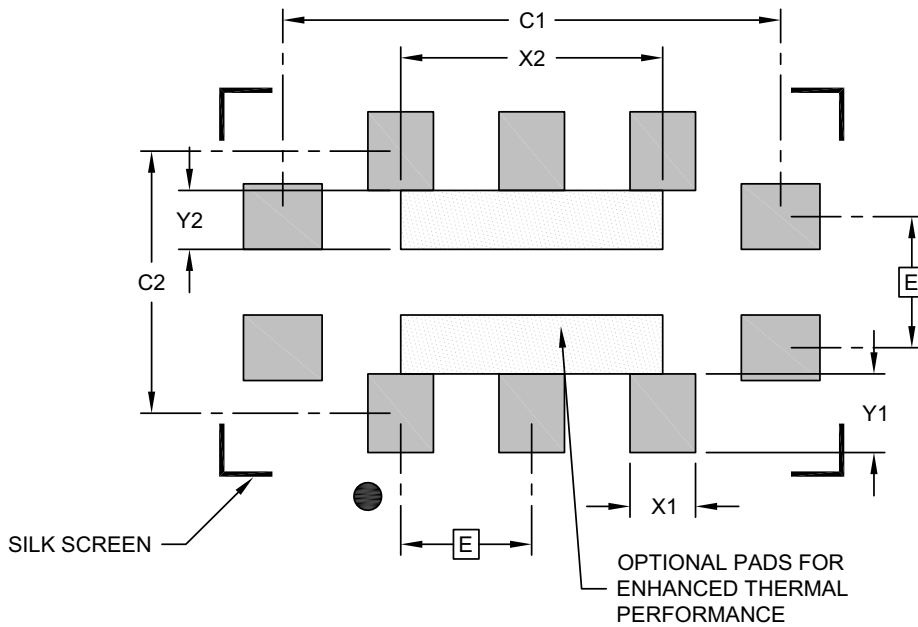
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1029 Rev A Sheet 2 of 2

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10-Lead Very Thin Plastic Quad Flat, No Lead Package (NDA) - 1.2x2.0x0.9 mm Body [VQFN]; Micrel Legacy Package FQFN1220-10LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width (X2)	X2			1.00
Optional Center Pad Length (X2)	Y2			0.225
Contact Pad Spacing	C1		1.90	
Contact Pad Spacing	C2		1.00	
Contact Pad Width (X10)	X1			0.25
Contact Pad Length (X10)	Y1			0.30
Contact Pad to Contact Pad (Xnn)	Y1	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3029 Rev A

APPENDIX A: REVISION HISTORY

Revision A (October 2020)

- Converted Micrel document MIC95410 to Microchip data sheet template DS20006431A.
- Minor grammatical text changes throughout.
- Typical Application Schematic, Bill of Materials, and the full PCB Layout Recommendations sections have been moved to the User's Guide for this device.

MIC95410

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Device</u>	<u>X</u>	<u>X</u>	<u>-XX</u>
Part No.	Temperature Range	Package	Media Type
Device:	MIC95410:	6.6 mΩ R _{DS(ON)} , 7A, 5.5V V _{IN} Load Switch	
Temperature Range:	Y =	-40°C to +125°C	
Package:	FL =	10-Lead VQFN	
Media Type:	T5 =	500/Reel	
	TR =	5,000/Reel	

Examples:

a) MIC95410YFL-T5: MIC95410, -40°C to +125°C, 10-Lead VQFN, 500/Reel

b) MIC95410YFL-TR: MIC95410, -40°C to +125°C, 10-Lead VQFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MIC95410

NOTES:

Note the following details of the code protection feature on Microchip devices:

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