MOSFET – N-Channel, POWERTRENCH®

30 V, 16.9 A, 5.7 mΩ

FDMC7672

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $R_{DS(on)}$ = 5.7 mΩ at V_{GS} = 10 V, I_D = 16.9 A
- Max $R_{DS(on)}$ = 7.0 mΩ at V_{GS} = 4.5 V, I_D = 15.0 A
- High Performance Technology for Extremely Low $R_{DS(on)}$
- Pb−Free, Halide Free and RoHS Compliant

Applications

- DC−DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	$\pm$20	V
I_D	Drain Current: Continuous, T_C = 25°C Continuous, T_A = 25°C (Note 1a) Pulsed	20 16.9 50	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	144	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	33 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
30 V	5.7 mΩ @ 10 V	16.9 A
	7.0 mΩ @ 4.5 V	
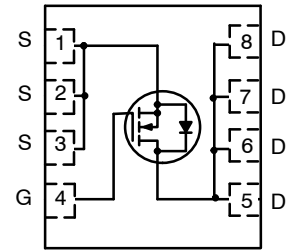
N-CHANNEL MOSFET
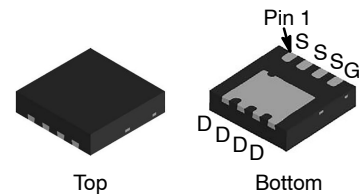
WDFN8 3.3 × 3.3, 0.65P
CASE 511DH

MARKING DIAGRAM
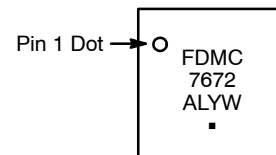
FDMC7672	= Specific Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week
▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
FDMC7672	WDFN8 (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	13	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C	–	–	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	1.9	3.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–6	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 16.9 A	–	4.3	5.7	mΩ
		V_{GS} = 4.5 V, I_D = 15.0 A	–	5.4	7.0	
		V_{GS} = 10 V, I_D = 16.9 A, T_J = 125°C	–	5.5	6.9	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 16.9 A	–	82	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	2925	3890	pF
C_{oss}	Output Capacitance		–	1050	1400	pF
C_{rss}	Reverse Transfer Capacitance		–	80	120	pF
R_g	Gate Resistance	f = 1 MHz	–	0.9	2.7	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 16.9 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	13	24	ns
t_r	Rise Time		–	6	12	ns
$t_{d(off)}$	Turn-Off Delay Time		–	31	49	ns
t_f	Fall Time		–	5	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 16.9 A	–	40	57	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 15 V, I_D = 16.9 A	–	18	24	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 16.9 A	–	9	–	nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 15 V, I_D = 16.9 A	–	4	–	nC

FDMC7672

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 16.9 A (Note 2)	–	0.83	1.2	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)	–	0.72	1.2	
t_{rr}	Reverse Recovery Time	I_F = 16.9 A, di/dt = 100 A/µs	–	39	62	ns
Q_{rr}	Reverse Recovery Charge		–	18	32	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{θJA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design.
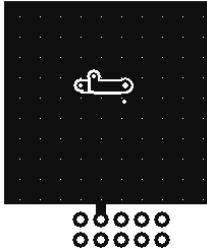
a) 53°C/W when mounted on a 1 in² pad of 2 oz copper.
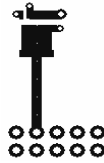
b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. E_{AS} of 144 mJ is based on starting $T_J = 25°C$, L = 1 mH, I_{AS} = 17 A, V_{DD} = 27 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T$_J$ = 25°C unless otherwise noted)
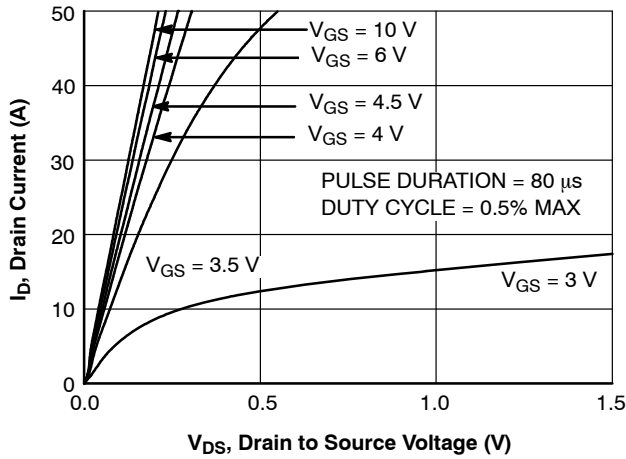
Figure 1. On−Region Characteristics
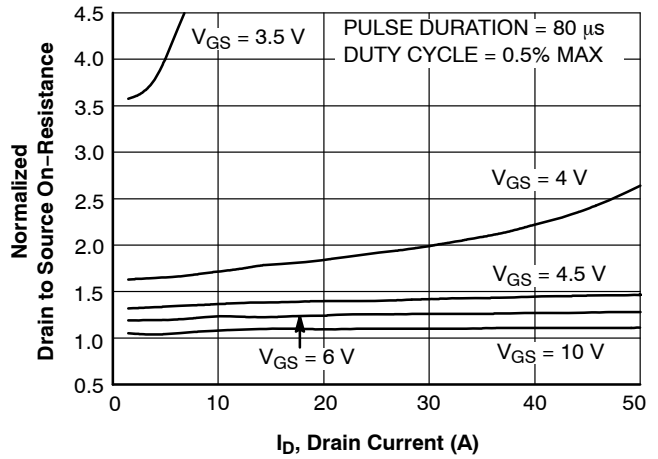
Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage
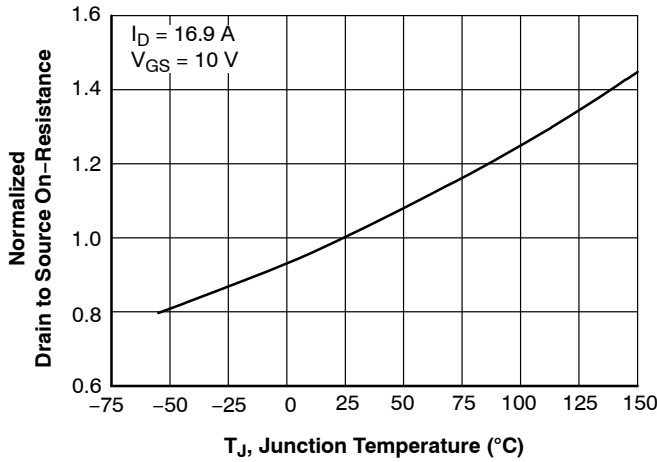
Figure 3. Normalized On−Resistance vs. Junction Temperature
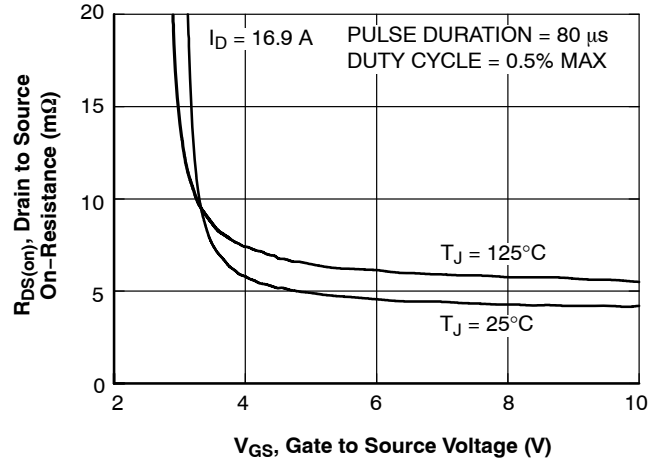
Figure 4. On−Resistance vs. Gate to Source Voltage
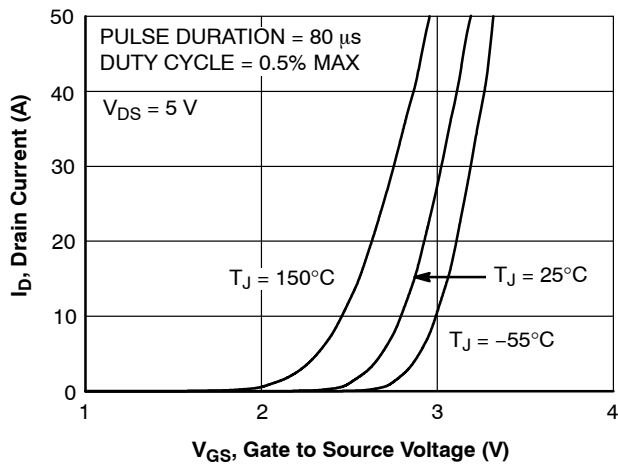
Figure 5. Transfer Characteristics
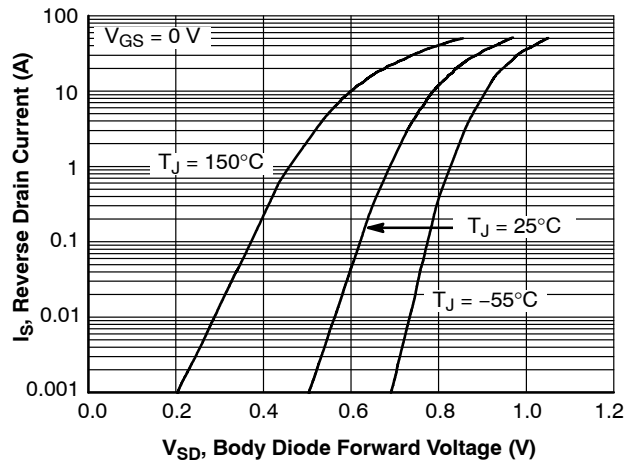
Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

$(T_J = 25°C$ unless otherwise noted)
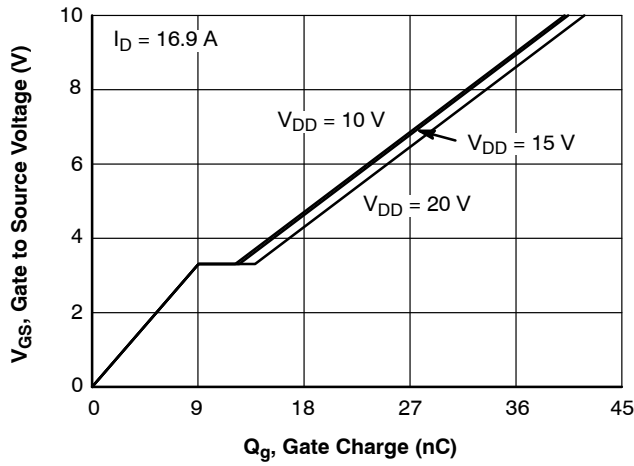
Figure 7. Gate Charge Characteristics
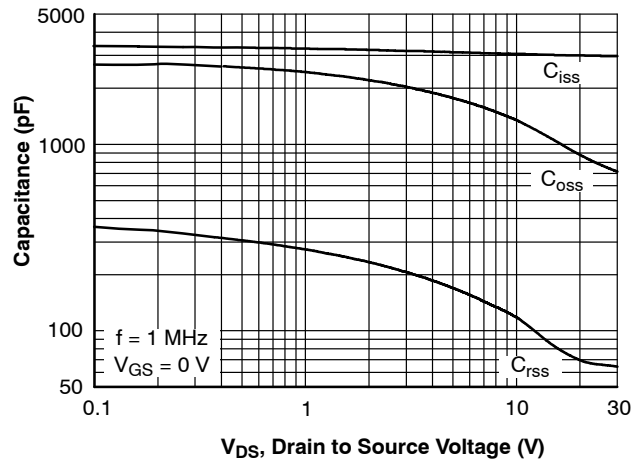
Figure 8. Capacitance vs. Drain to Source Voltage
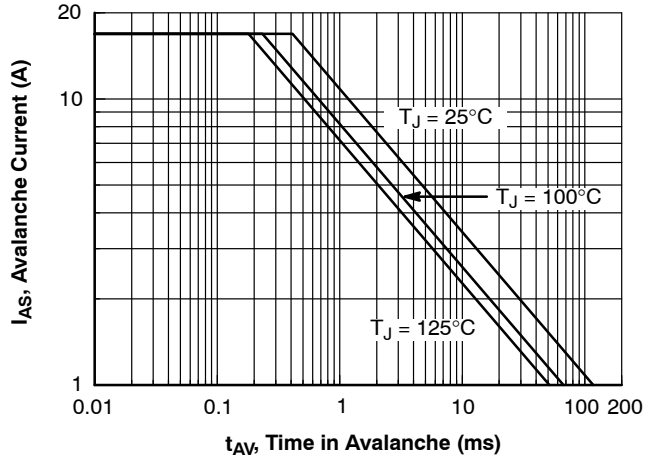
Figure 9. Unclamped Inductive Switching Capability
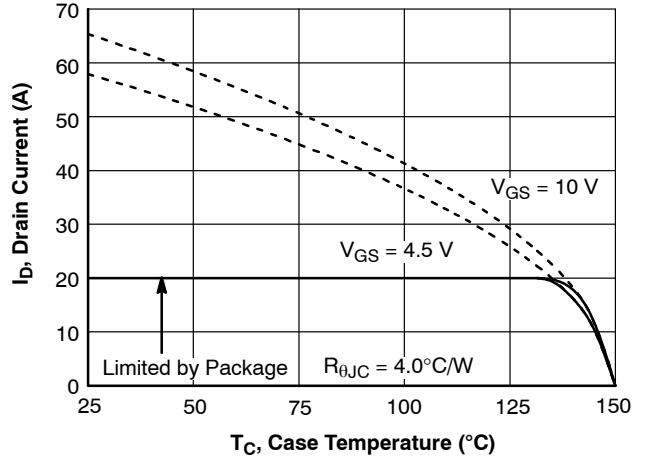
Figure 10. Maximum Continuous Drain Current vs. Case Temperature
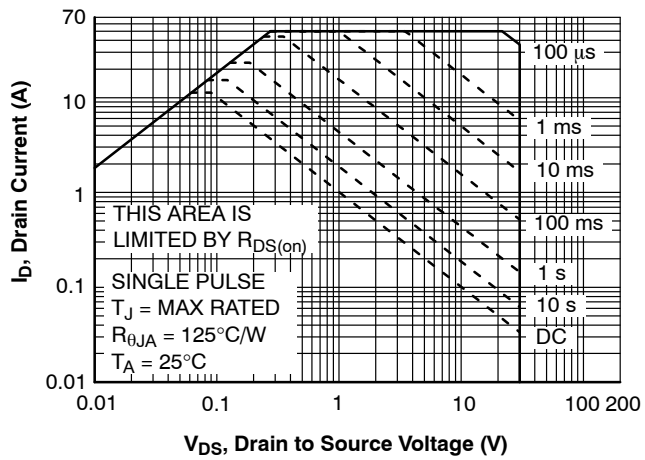
Figure 11. Forward Bias Safe Operating Area
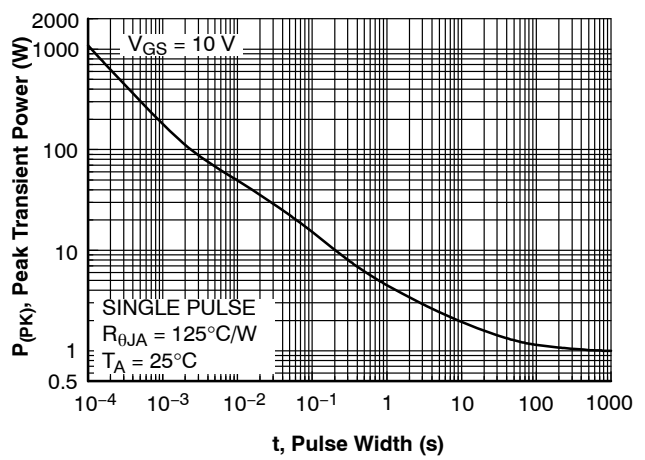
Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)
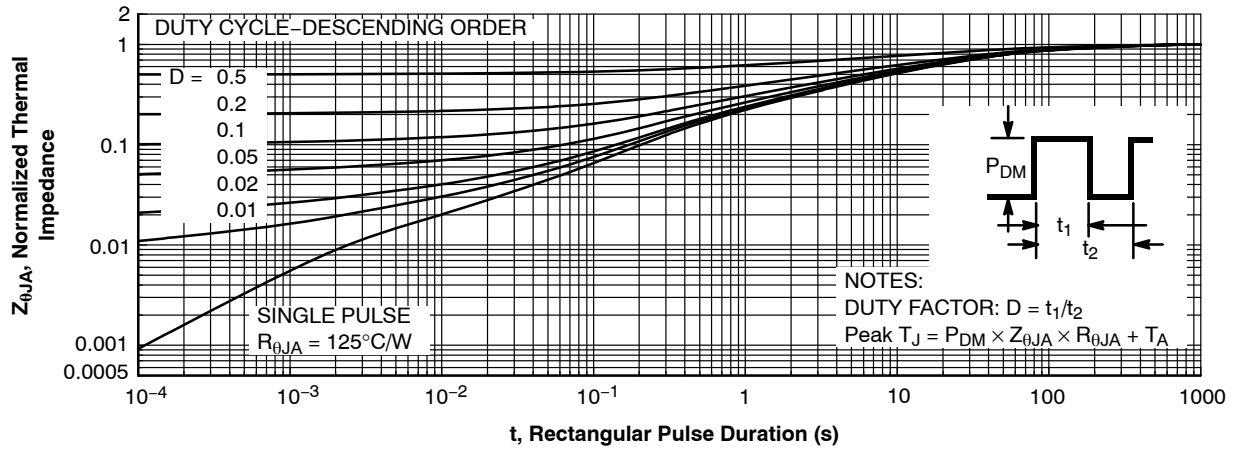
Figure 13. Transient Thermal Response Curve

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ISSUE O

DATE 31 JUL 2016

TOP VIEW

PIN#1 IDENT

SIDE VIEW

SEATING PLANE
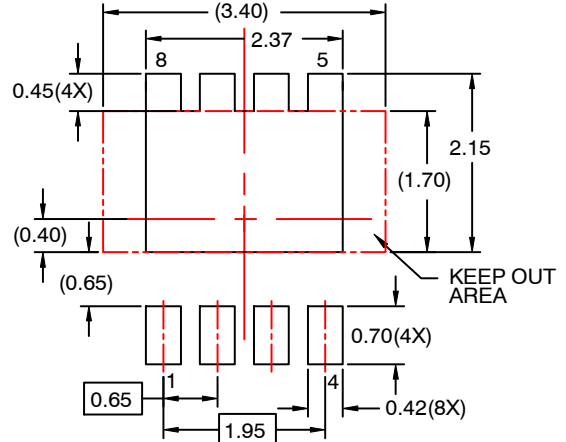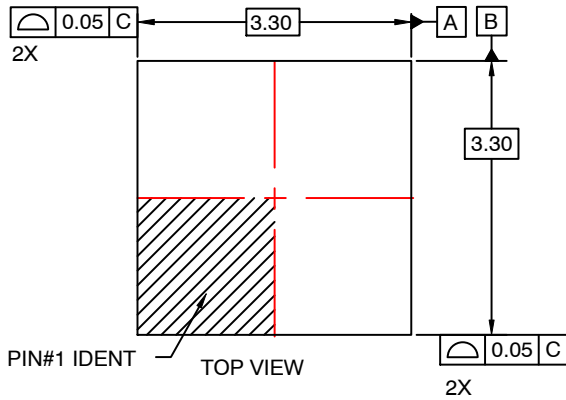
BOTTOM VIEW

RECOMMENDED LAND PATTERN

KEEP OUT AREA

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
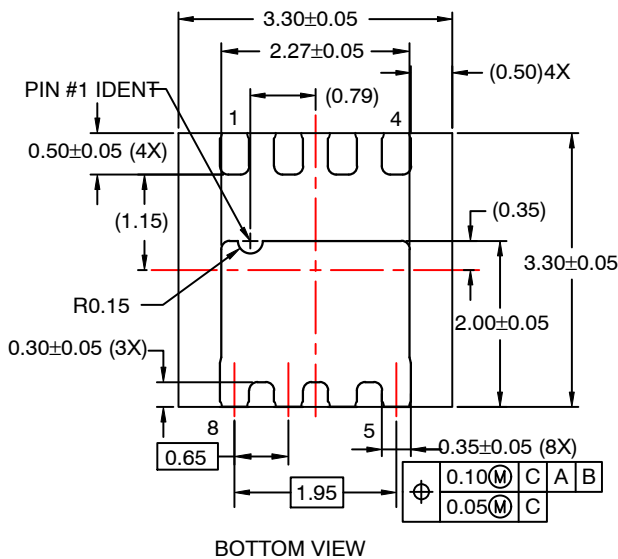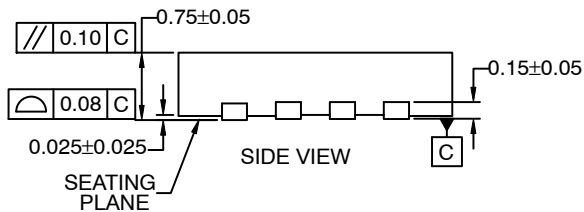
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ADDITIONAL INFORMATION

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