- **8-Bit Voltage Output DAC**
- **Programmable Settling Time vs Power Consumption**
  - **3 μs in Fast Mode**
  - **9 μs in Slow Mode**
- **Ultra Low Power Consumption:**
  - **900 μW Typ in Slow Mode at 3 V**
  - **2.1 mW Typ in Fast Mode at 3 V**
- **Differential Nonlinearity . . . <0.2 LSB**
- **Compatible With TMS320 and SPI Serial Ports**
- **Power-Down Mode**
- **Buffered High-Impedance Reference Input**
- **Monotonic Over Temperature**
- **Available in MSOP Package**

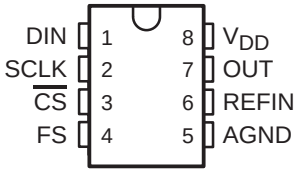
applications

- **Digital Servo Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

description

The TLV5623 is a 8-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5623 is programmed with a 16-bit serial string containing 4 control and 8 data bits. Developed for a wide range of supply voltages, the TLV5623 can operate from 2.7 V to 5.5 V.

D OR DGK PACKAGE
(TOP VIEW)



The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFIN terminal to reduce the need for a low source impedance drive to the terminal.

Implemented with a CMOS process, the TLV5623 is designed for single supply operation from 2.7 V to 5.5 V. The device is available in an 8-terminal SOIC package. The TLV5623C is characterized for operation from 0°C to 70°C. The TLV5623I is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE† (D)	MSOP (DGK)
0°C to 70°C	TLV5623CD	TLV5623CDGK
−40°C to 85°C	TLV5623ID	TLV5623IDGK

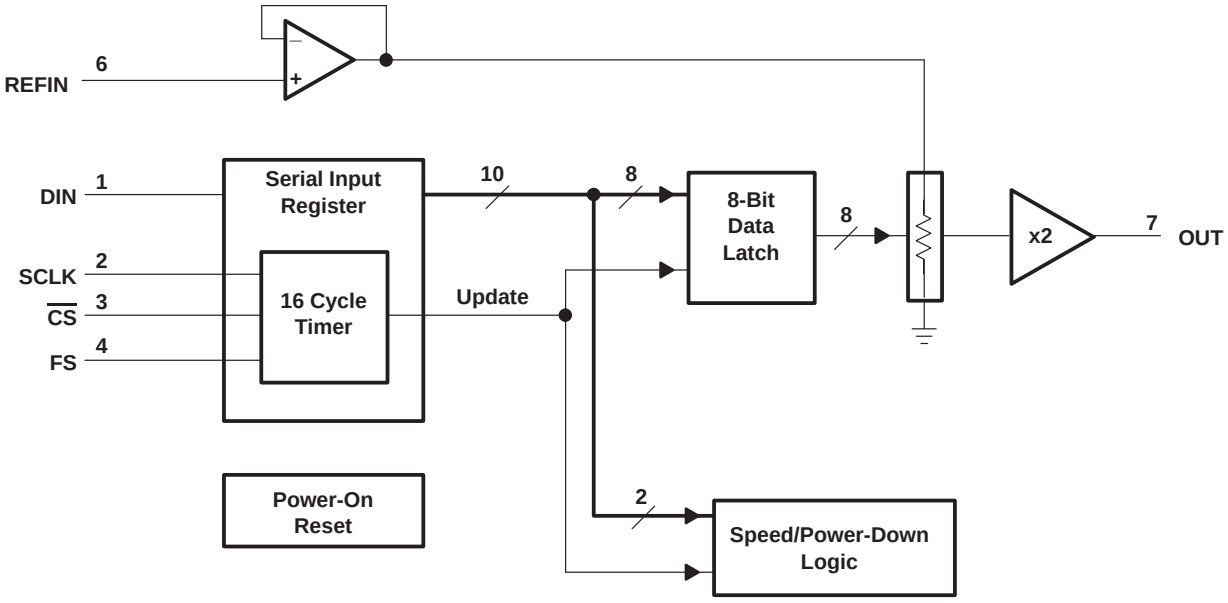
† Available in tape and reel as the TLV5623CDR and the TLV5623IDR

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002 − 2004, Texas Instruments Incorporated

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	5		Analog ground
$\overline{CS}$	3	I	Chip select. Digital input used to enable and disable inputs, active low.
DIN	1	I	Serial digital data input
FS	4	I	Frame sync. Digital input used for 4-wire serial interfaces such as the TMS320 DSP interface.
OUT	7	O	DAC analog output
REFIN	6	I	Reference analog input voltage
SCLK	2	I	Serial digital clock input
V_{DD}	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . . . 7 V
Reference input voltage range . . . . . − 0.3 V to V_{DD} + 0.3 V
Digital input voltage range . . . . . − 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5623C . . . . . 0°C to 70°C
TLV5623I . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V	2			V
	DV_{DD} = 5.5 V	2.4			V
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V			0.6	V
	DV_{DD} = 5.5 V			1	V
Reference voltage, V_{ref} to REFIN terminal	V_{DD} = 5 V (see Note 1)	AGND	2.048	V_{DD} −1.5	V
Reference voltage, V_{ref} to REFIN terminal	V_{DD} = 3 V (see Note 1)	AGND	1.024	V_{DD} −1.5	V
Load resistance, R_L		2	10		kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				20	MHz
Operating free-air temperature, T_A	TLV5623C	0		70	°C
	TLV5623I	−40		85	°C

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ $V_{DD/2}$ causes clipping of the transfer function.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

power supply

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current		V_{DD} = 5 V, VREF = 2.048 V, No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		0.9	1.35	mA
				Slow		0.4	0.6	mA
			V_{DD} = 3 V, VREF = 1.024 V No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		0.7	1.1	mA
				Slow		0.3	0.45	mA
	Power down supply current (see Figure 12)					1		µA
PSRR	Power supply rejection ratio	Zero scale	See Note 2			−68		dB
		Full scale	See Note 3			−68		
	Power on threshold voltage, POR					2		V

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
PSRR = 20 log [(E_{ZS}(V_{DD}max) − E_{ZS}(V_{DD}min))/V_{DD}max]
3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
PSRR = 20 log [(E_G(V_{DD}max) − E_G(V_{DD}min))/V_{DD}max]

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

static DAC specifications R_L = 10 kΩ, C_L = 100 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8			bits
INL	Integral nonlinearity	See Note 4		±0.3	±0.5	LSB
DNL	Differential nonlinearity	See Note 5		±0.07	±0.2	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See Note 6			±10	mV
$E_{ZS\ TC}$	Zero-scale-error temperature coefficient	See Note 7		10		ppm/°C
E_G	Gain error	See Note 8			±0.6	% of FS voltage
	Gain-error temperature coefficient	See Note 9		10		ppm/°C

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 10 to code 255.
5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 10 to code 255.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: $E_{ZS}\ TC = [E_{ZS}\ (T_{max}) - E_{ZS}\ (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
8. Gain error is the deviation from the ideal output ($2V_{ref}$ − 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
9. Gain temperature coefficient is given by: $E_G\ TC = [E_G(T_{max}) - E_G\ (T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.

output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ	0		V_{DD}−0.1	V
	Output load regulation accuracy	R_L = 2 kΩ, vs 10 kΩ		±0.1	±0.25	% of FS voltage

reference input (REF)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		V_{DD}−1.5	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REFIN = 0.2 V_{pp} + 1.024 V dc	Slow		525		kHz
			Fast		1.3		MHz
	Reference feed through	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 10)			−75		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±1	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±1	µA
C_I	Input capacitance			3		pF

operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF, See Note 11	Fast		3	5.5	µs
			Slow		9	20	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ, C_L = 100 pF, See Note 12	Fast		1		µs
			Slow		2		µs
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, See Note 13	Fast		3.6		V/µs
			Slow		0.9		
	Glitch energy	Code transition from 0x7F0 to 0x800			10		nV−s
S/N	Signal to noise	fs = 400 KSPS fout = 1.1 kHz, R_L = 10 kΩ, C_L = 100 pF, BW = 20 kHz			57		dB
S/(N+D)	Signal to noise + distortion				49		dB
THD	Total harmonic distortion				−50		dB
	Spurious free dynamic range				60		dB

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFF0 or 0xFF0 to 0x020. Not tested, ensured by design.
12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, ensured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su(CS-FS)}$	Setup time, $\overline{CS}$ low before FS↓	10			ns
$t_{su(FS-CK)}$	Setup time, FS low before first negative SCLK edge	8			ns
$t_{su(C16-FS)}$	Setup time, sixteenth negative edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
$t_{su(C16-CS)}$	Setup time, sixteenth positive SCLK edge (first positive after D0 is sampled) before $\overline{CS}$ rising edge. If FS is used instead of the sixteenth positive edge to update the DAC, then the setup time is between the FS rising edge and $\overline{CS}$ rising edge.	10			ns
t_{wH}	Pulse duration, SCLK high	25			ns
t_{wL}	Pulse duration, SCLK low	25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	Pulse duration, FS high	20			ns

PARAMETER MEASUREMENT INFORMATION

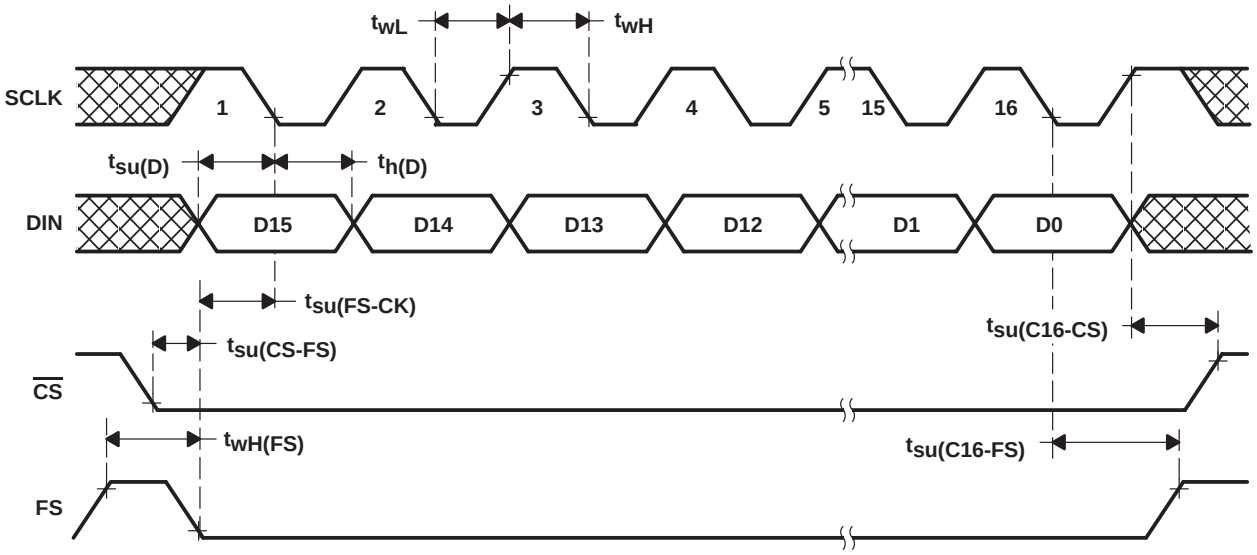


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
LOAD CURRENT

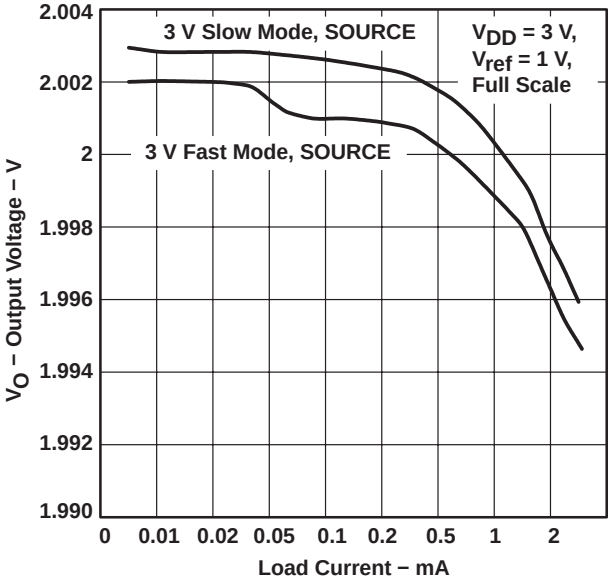


Figure 2

OUTPUT VOLTAGE
vs
LOAD CURRENT

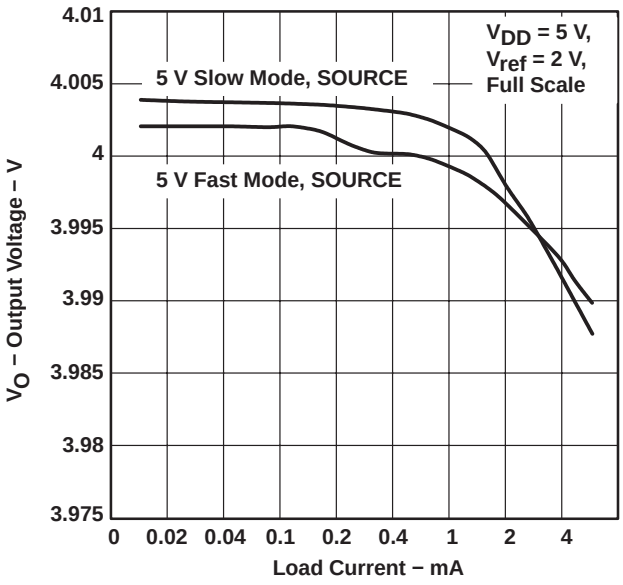


Figure 3

OUTPUT VOLTAGE
vs
LOAD CURRENT

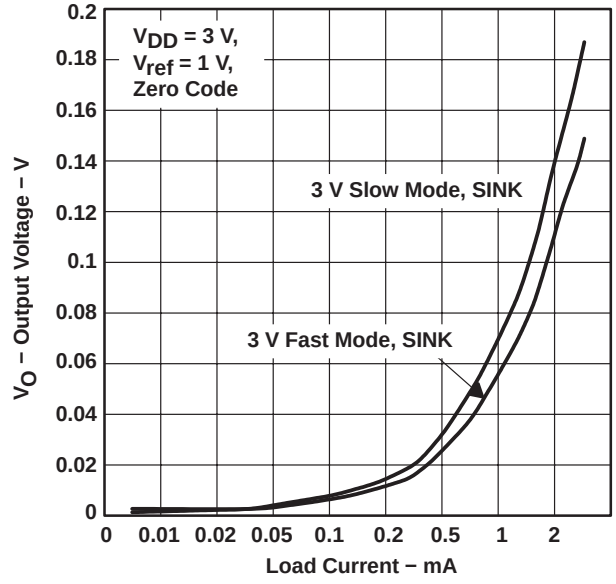


Figure 4

OUTPUT VOLTAGE
vs
LOAD CURRENT

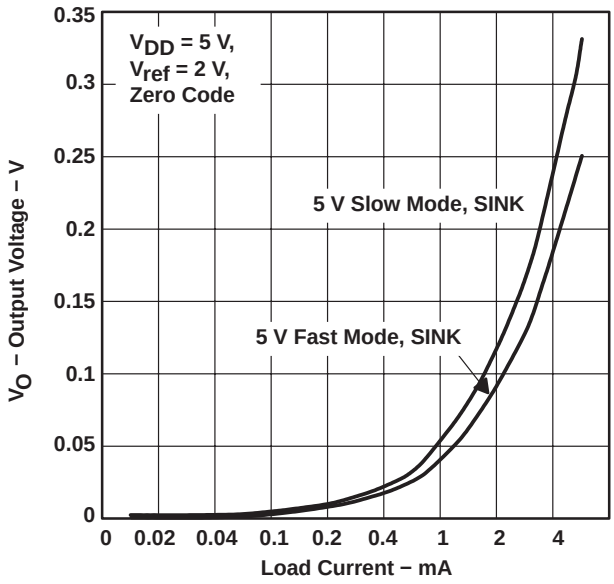


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

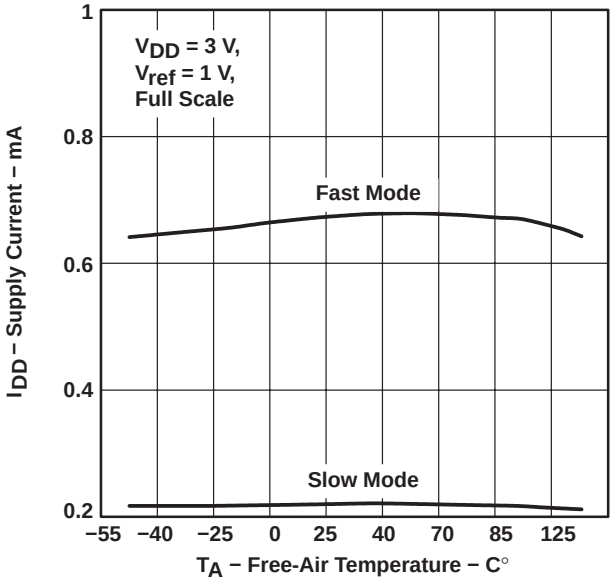


Figure 6

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

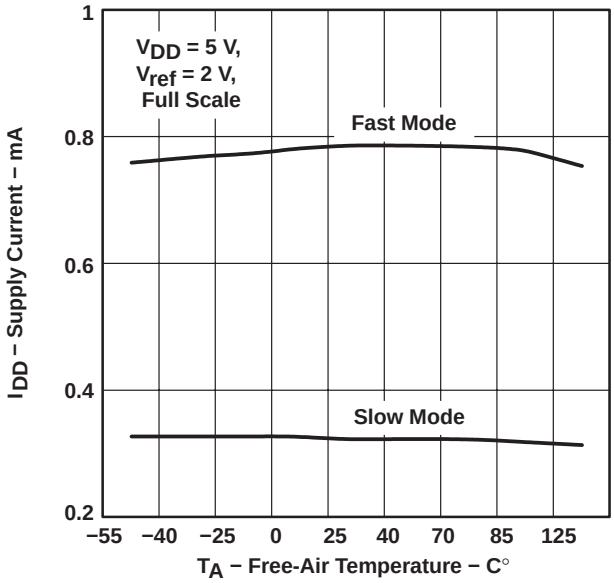


Figure 7

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

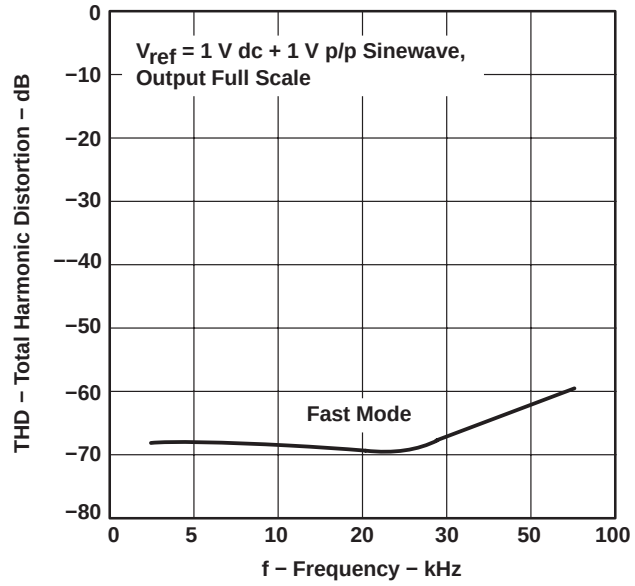


Figure 8

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

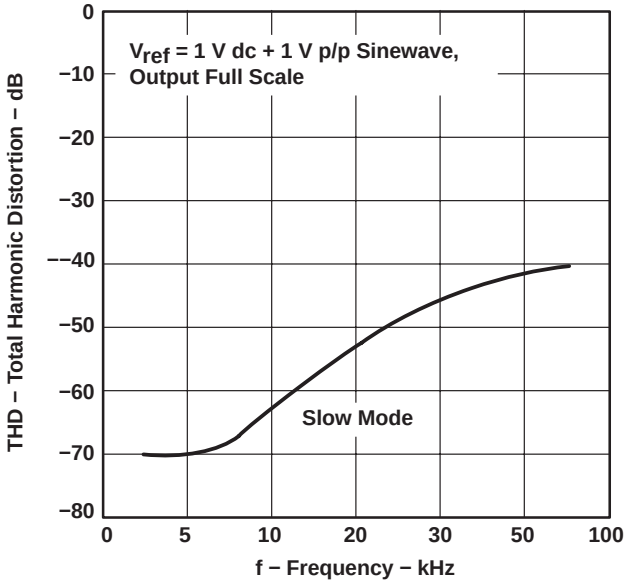


Figure 9

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

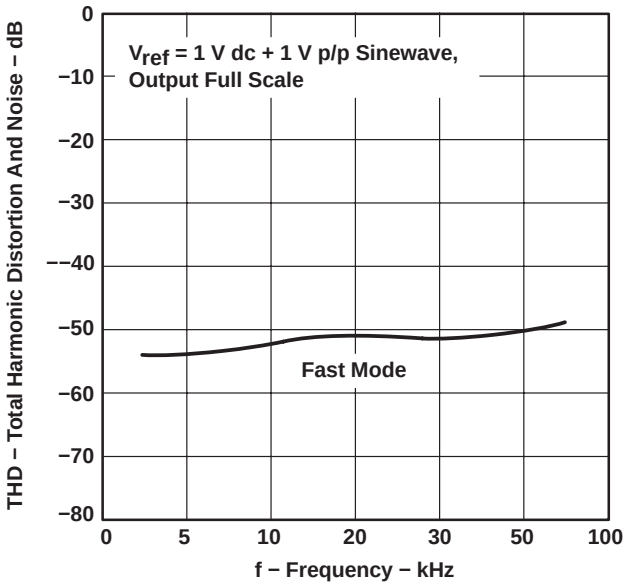


Figure 10

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

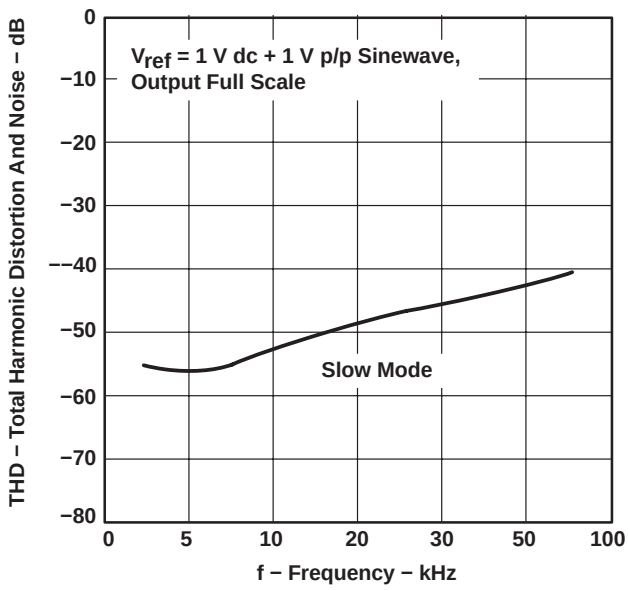


Figure 11

SUPPLY CURRENT
vs
TIME (WHEN ENTERING POWER-DOWN MODE)

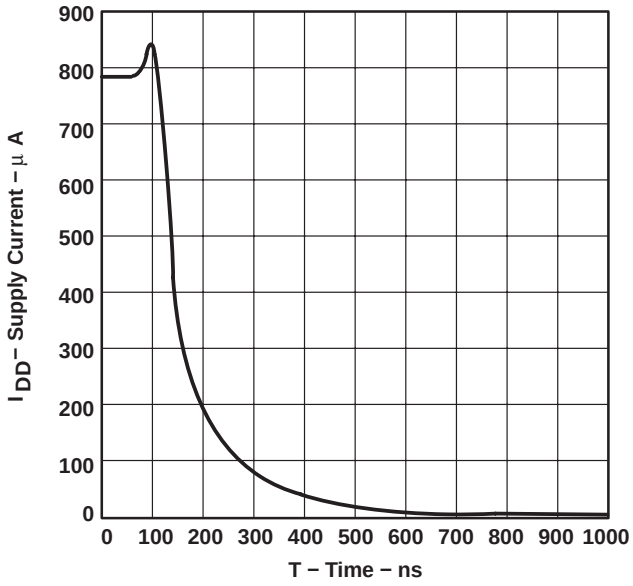


Figure 12

TYPICAL CHARACTERISTICS

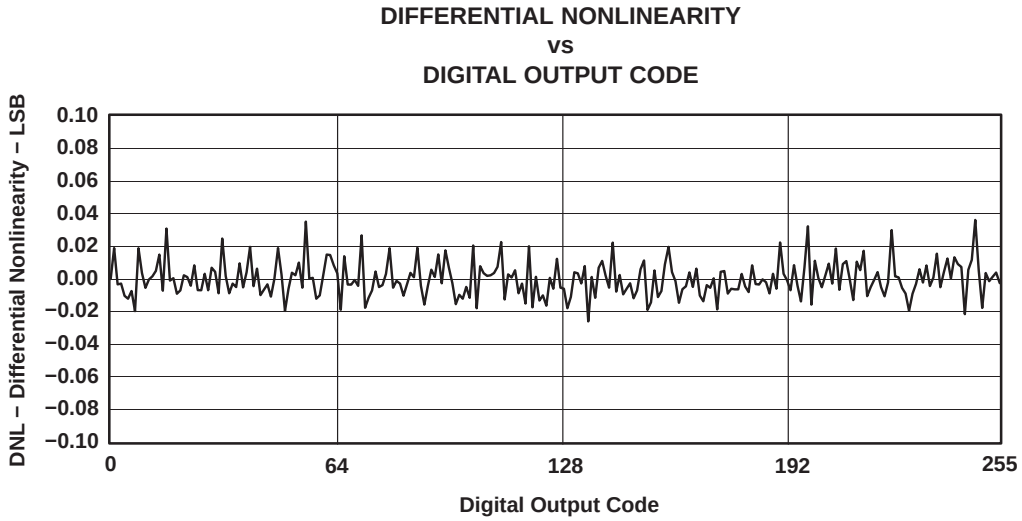


Figure 13

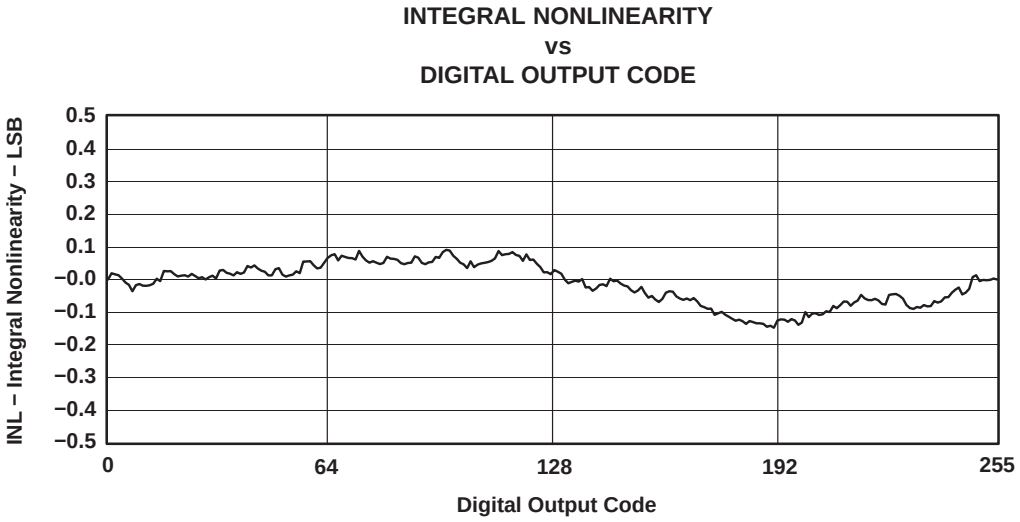


Figure 14

APPLICATION INFORMATION

general function

The TLV5623 is an 8-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{2^n}\ [\mathrm{V}]$$

where REF is the reference voltage and CODE is the digital input value within the range of 0_{10} to 2^{n-1}, where n = 8 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

The device has to be enabled with $\overline{\mathrm{CS}}$ set to low. A falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch, which updates the voltage output to the new level.

The serial interface of the TLV5623 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four-wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320 family. Figure 15 shows an example with two TLV5623s connected directly to a TMS320 DSP.

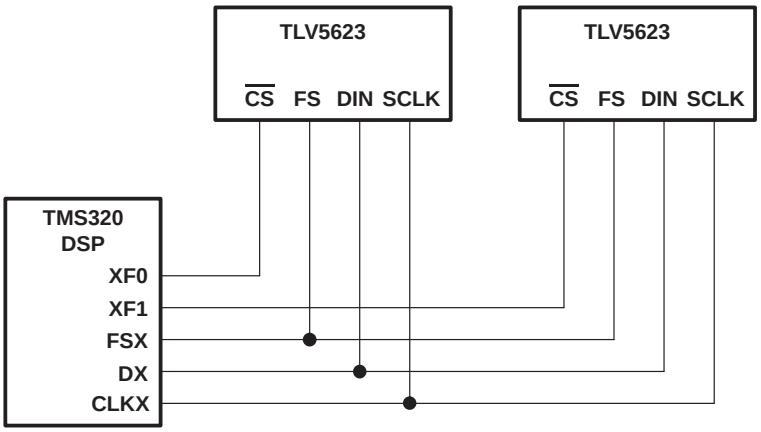


Figure 15. TMS320 Interface

APPLICATION INFORMATION

serial interface (continued)

If there is no need to have more than one device on the serial bus, then $\overline{CS}$ can be tied low. Figure 16 shows an example of how to connect the TLV5623 to a TMS320, SPI, or Microwire port using only three pins.

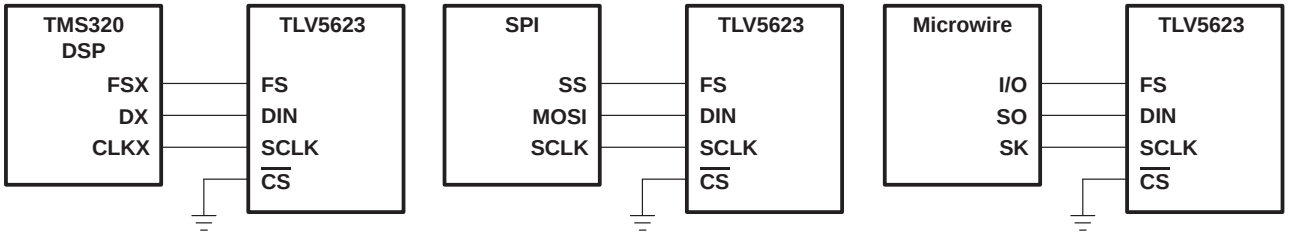


Figure 16. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5623. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{SCLKmax} = \frac{1}{t_{wH(min)} + t_{wL(min)}} = 20\ \text{MHz}$$

The maximum update rate is:

$$f_{UPDATEmax} = \frac{1}{16\left(t_{wH(min)} + t_{wL(min)}\right)} = 1.25\ \text{MHz}$$

The maximum update rate is a theoretical value for the serial interface, since the settling time of the TLV5623 has to be considered also.

data format

The 16-bit data word for the TLV5623 consists of two parts:

- Control bits (D15 . . . D12)
- New DAC value (D11 . . . D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	SPD	PWR	X	New DAC value (8 bits)								0	0	0	0

X: don't care
SPD: Speed control bit. 1 → fast mode 0 → slow mode
PWR: Power control bit. 1 → power down 0 → normal operation

In power-down mode, all amplifiers within the TLV5623 are disabled.

APPLICATION INFORMATION

TLV5623 interfaced to TMS320C203 DSP

hardware interfacing

Figure 17 shows an example how to connect the TLV5623 to a TMS320C203 DSP. The serial interface of the TLV5623 is ideally suited to this configuration, using a maximum of four wires to make the necessary connections. In applications where only one synchronous serial peripheral is used, the interface can be simplified even further by pulling $\overline{CS}$ low all the time as shown in the figure.

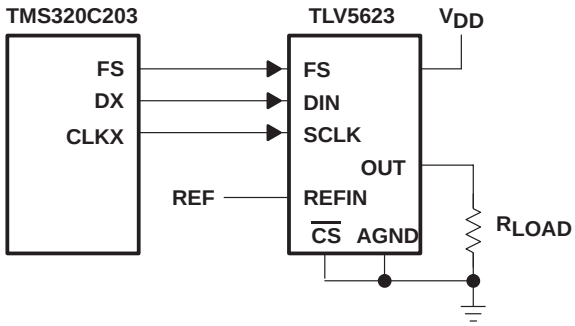


Figure 17. TLV5623 to DSP Interface

TLV5623 interfaced to MCS51® microcontroller

hardware interfacing

Figure 18 shows an example of how to connect the TLV5623 to an MCS51® compatible microcontroller. The serial DAC input data and external control signals are sent via I/O port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the TxD line. P3.4 and P3.5 are configured as outputs to provide the chip select and frame sync signals for the TLV5623.

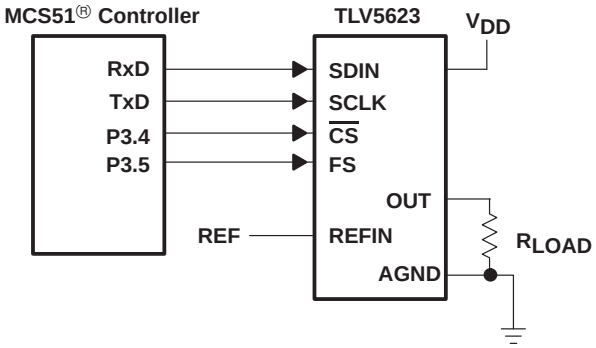


Figure 18. TLV5623 to MCS51® Controller Interface

MCS is a registered trademark of Intel Corporation

APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 19.

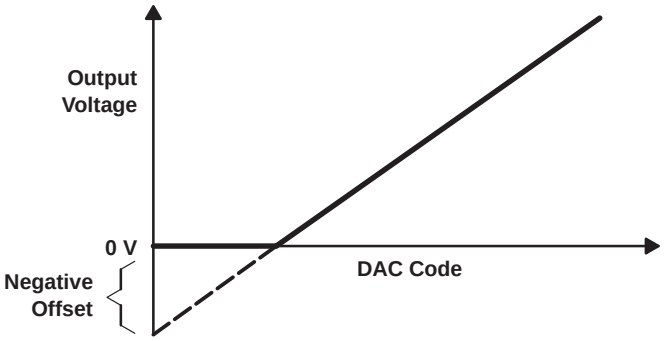


Figure 19. Effect of Negative Offset (single supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1-μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 20 shows the ground plane layout and bypassing technique.

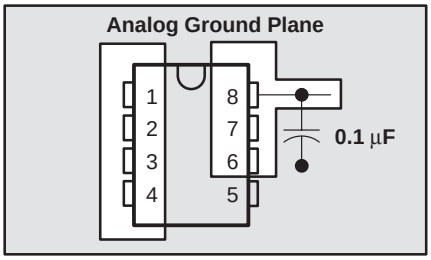


Figure 20. Power-Supply Bypassing

APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5623CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5623	Samples
TLV5623CDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADT	Samples
TLV5623CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ADT	Samples
TLV5623CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5623	Samples
TLV5623ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5623	Samples
TLV5623IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADU	Samples
TLV5623IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADU	Samples
TLV5623IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5623	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

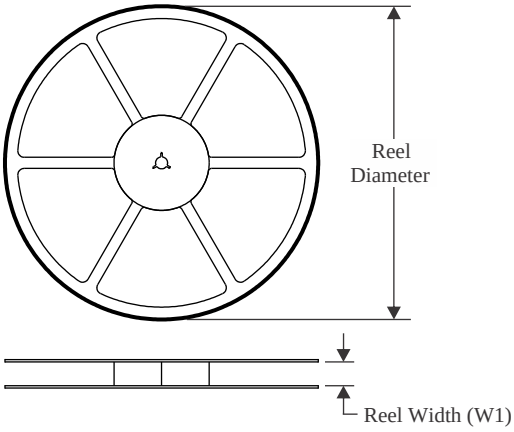
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

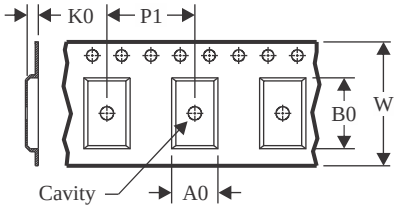
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

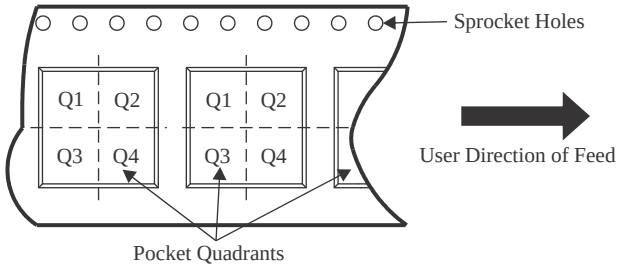


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

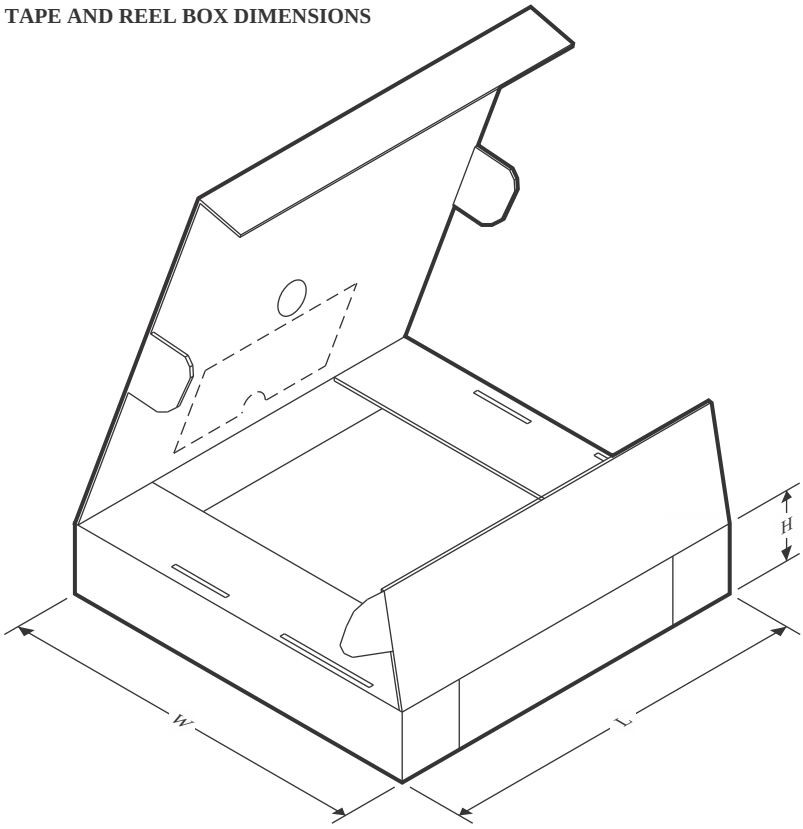
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5623CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV5623CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV5623IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV5623IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

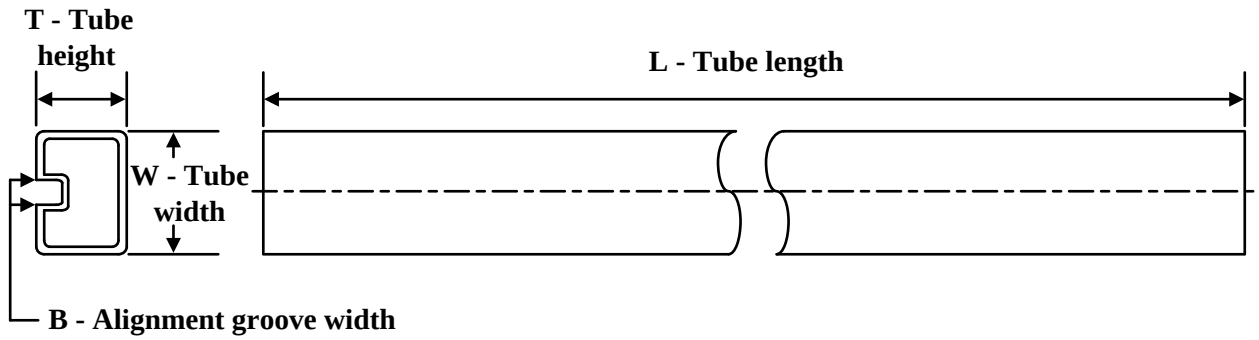
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

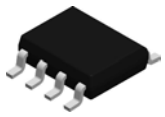
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5623CDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLV5623CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLV5623IDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
TLV5623IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5623CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV5623CDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
TLV5623ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV5623IDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88

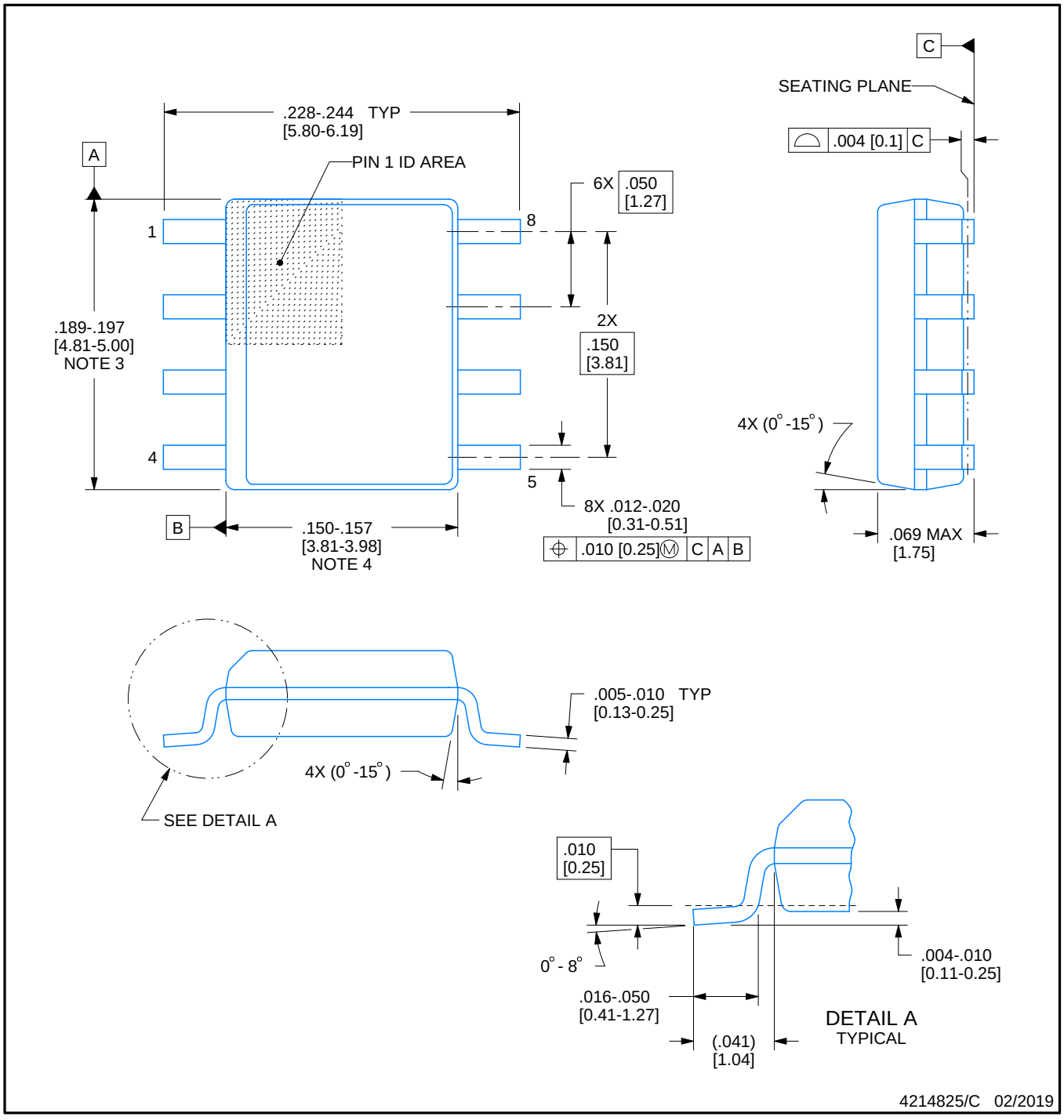


PACKAGE OUTLINE

D0008A

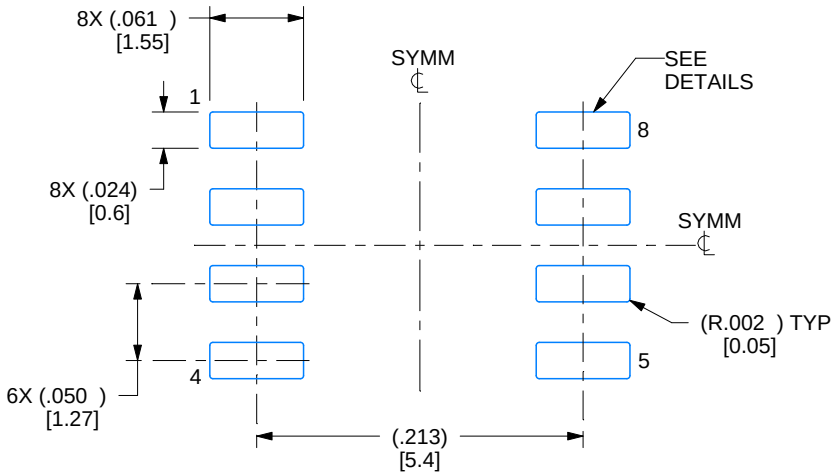
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

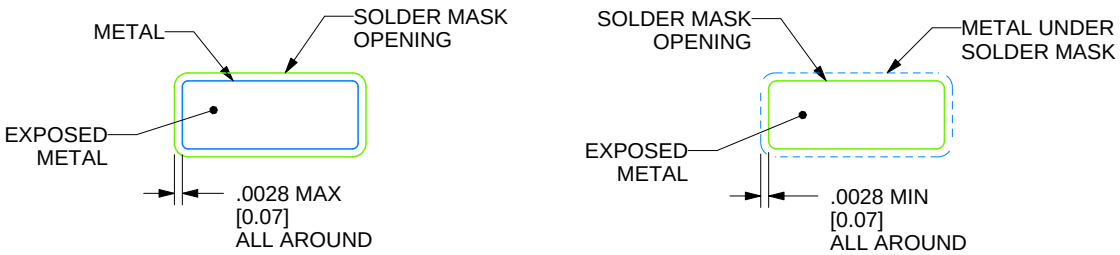


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

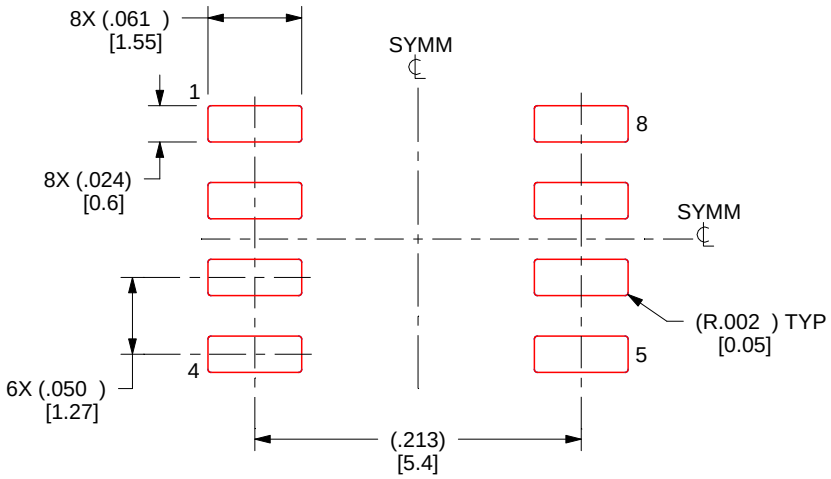
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



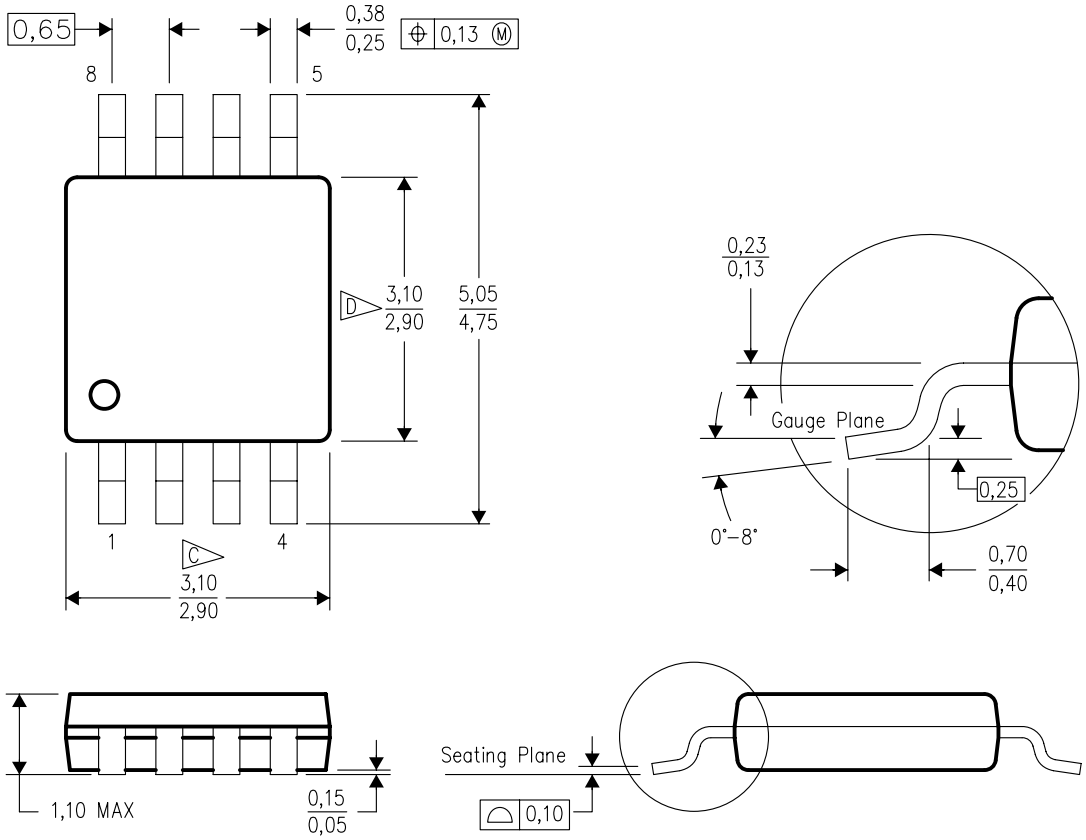
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

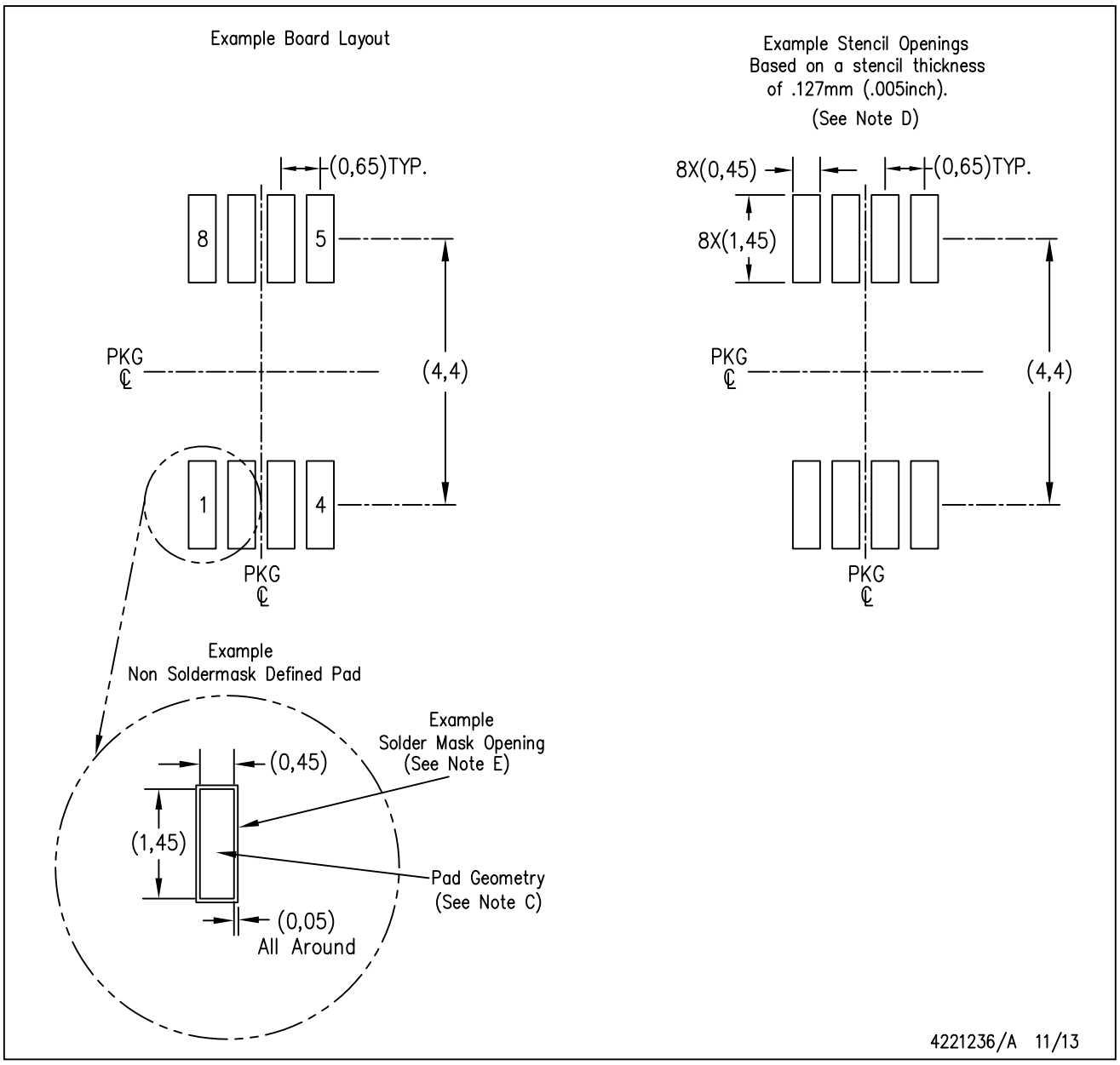
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated