



Customer Information Notification

2020020271

Issue Date: 14-Mar-2020
Effective Date: 15-Mar-2020

Here's your personalized quality information concerning products Digi-Key purchased from NXP. For detailed information we invite you to view this notification online



QUALITY

This notice is NXP Company Proprietary.

Change Category

- | | | | | |
|--|---|--|---|---|
| <input type="checkbox"/> Wafer Fab Process | <input type="checkbox"/> Assembly Process | <input type="checkbox"/> Product Marking | <input type="checkbox"/> Test Location | <input type="checkbox"/> Design |
| <input type="checkbox"/> Wafer Fab Materials | <input type="checkbox"/> Assembly Materials | <input type="checkbox"/> Mechanical Specification | <input type="checkbox"/> Test Process | <input type="checkbox"/> Errata |
| <input type="checkbox"/> Wafer Fab Location | <input type="checkbox"/> Assembly Location | <input type="checkbox"/> Packing/Shipping/Labeling | <input type="checkbox"/> Test Equipment | <input type="checkbox"/> Electrical spec./Test coverage |
| <input type="checkbox"/> Firmware | <input checked="" type="checkbox"/> Other - Datasheet correction and update | | | |

MPC5746R Data Sheet Updates To Rev.7

Description

NXP Semiconductors announces data sheet update for the MPC5746R from revision 6 to revision 7. The revision history included in the updated document provides a details description of the changes.

Data sheet changes:

- Page 37: In Table 20, changed the condition of dGROUP from "Within pass band - Tclk is $f_{ADCD_M} / 2$ " to "Within pass band - Tclk is $2/f_{ADCD_M}$ ".
- Page 39: In the footnote (no.13) of tLATENCY, changed the Register Latency formula from "REGISTER LATENCY= $tLATENCY + 0.5/f_{ADCD_S} + 2 (~+1)/f_{ADCD_M} + 2(~+1)f_{PBRIDGE_CLK}$ where f_{ADCD_S} is the frequency of the sampling clock, f_{ADCD_M} is the frequency of the modulator" to "REGISTER LATENCY = $tLATENCY + 0.5/f_{ADCD_S} + 2 (~+1)/f_{ADCD_M} + 2(~+1)/f_{PBRIDGE_CLK}$ where f_{ADCD_S} is the after-decimation ADC output data rate, $f_{ADCD_M}/2$ is the modulator sampling rate and $f_{PBRIDGE_CLK}$ is the frequency of the peripheral bridge clock feeds to the ADC S/D module".

The MPC5746R data sheet revision 7 is attached to this notice and can be found at:
https://www.nxp.com/products/processors-and-microcontrollers/power-architecture/mpc55xx-5xxx-mcus/ultra-reliable-mpc57xx-mcus/automotive-industrial-engine-management-mcu:MPC5746R?tab=Documentation_Tab

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DS-02.

Reason

The data sheet has been updated to correct errors and / or provide additional technical clarification on some device features.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.

Data Sheet Revision

A new datasheet will be issued

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

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Affected Part Numbers

SPC5743RK1MLU5

SPC5746RK1MMT5