

# MSB1218A-RT1G

## PNP Silicon General Purpose Amplifier Transistor

This PNP Silicon Epitaxial Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC-70/SOT-323 package which is designed for low power surface mount applications.

### Features

- High  $h_{FE}$ , 210 - 460
- Low  $V_{CE(sat)}$ ,  $< 0.5$  V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	45	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	45	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current - Continuous	$I_C$	100	mAdc
Collector Current - Peak	$I_{C(P)}$	200	mAdc

### THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Power Dissipation (Note 1)	$P_D$	150	mW
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector-Emitter Breakdown Voltage ( $I_C = 2.0$ mAdc, $I_B = 0$ )	$V_{(BR)CEO}$	45	-	Vdc
Collector-Base Breakdown Voltage ( $I_C = 10$ $\mu\text{Adc}$ , $I_E = 0$ )	$V_{(BR)CBO}$	45	-	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10$ $\mu\text{Adc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	7.0	-	Vdc
Collector-Base Cutoff Current ( $V_{CB} = 20$ Vdc, $I_E = 0$ )	$I_{CBO}$	-	0.1	$\mu\text{A}$
Collector-Emitter Cutoff Current ( $V_{CE} = 10$ Vdc, $I_B = 0$ )	$I_{CEO}$	-	100	$\mu\text{A}$
DC Current Gain (Note 2) ( $V_{CE} = 10$ Vdc, $I_C = 2.0$ mAdc)	$h_{FE1}$	210	340	-
Collector-Emitter Saturation Voltage (Note 2) ( $I_C = 100$ mAdc, $I_B = 10$ mAdc)	$V_{CE(sat)}$	-	0.5	Vdc

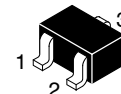
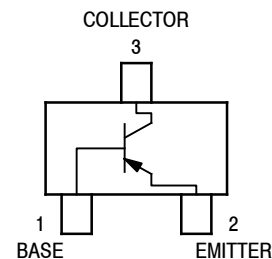
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.
2. Pulse Test: Pulse Width  $\leq 300$   $\mu\text{s}$ , D.C.  $\leq 2\%$ .



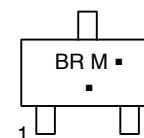
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SC-70 (SOT-323)  
CASE 419  
STYLE 4

### MARKING DIAGRAM



BR = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)  
\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
MSB1218A-RT1G	SC-70 (Pb-Free)	3000 /Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MSB1218A-RT1G

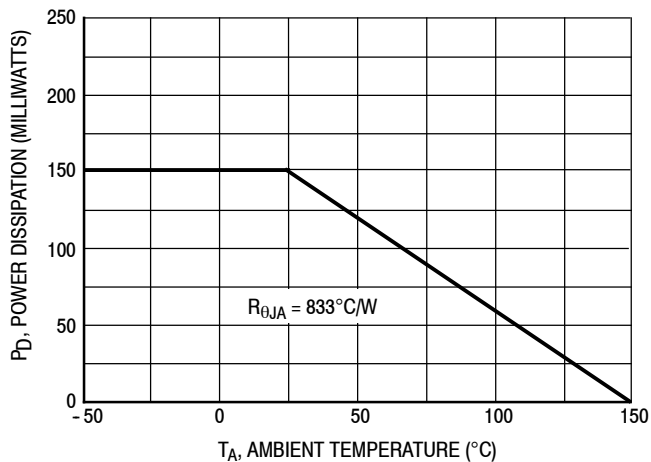


Figure 1. Derating Curve

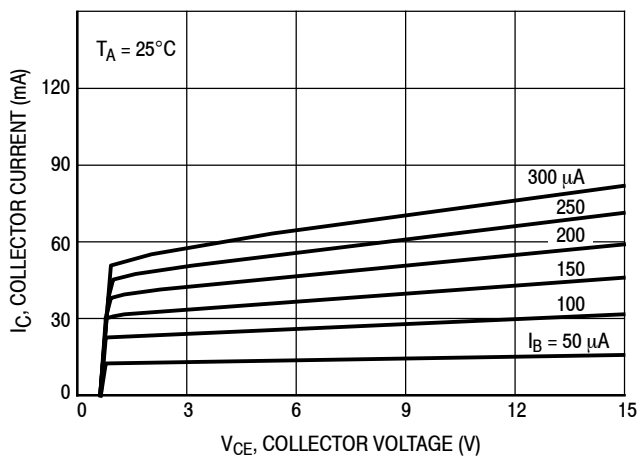


Figure 2. I<sub>C</sub> - V<sub>CE</sub>

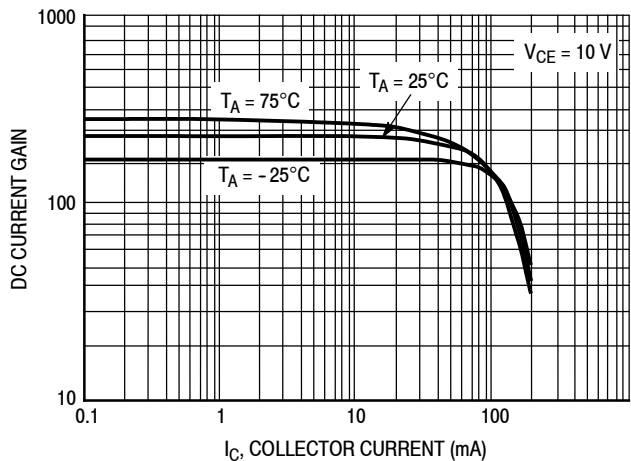


Figure 3. DC Current Gain

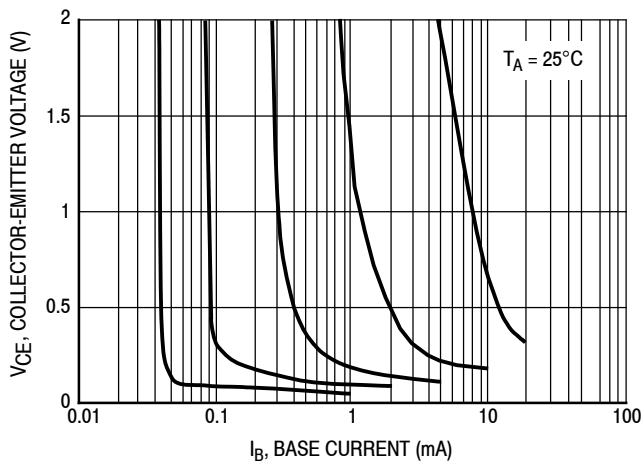


Figure 4. Collector Saturation Region

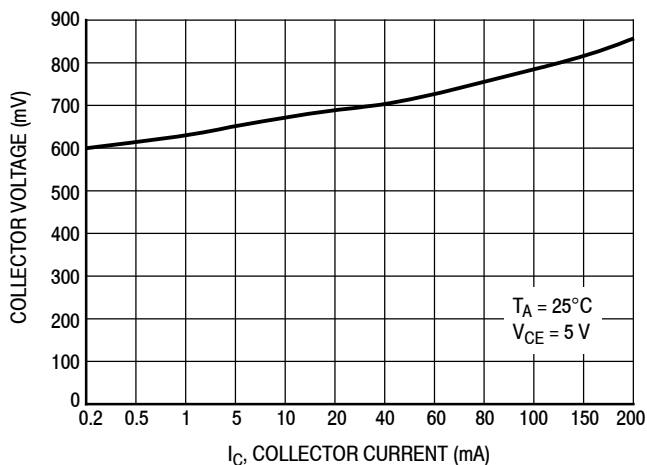


Figure 5. On Voltage

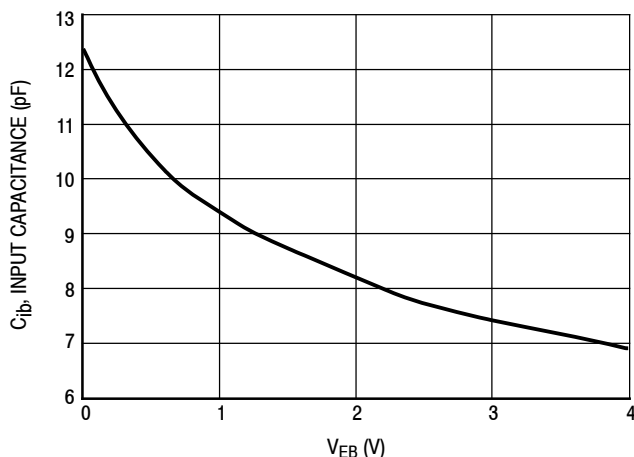


Figure 6. Capacitance

# MSB1218A-RT1G

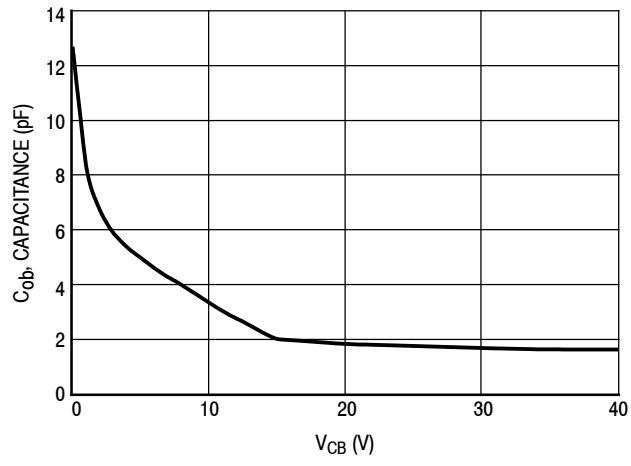
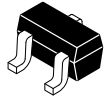


Figure 7. Capacitance

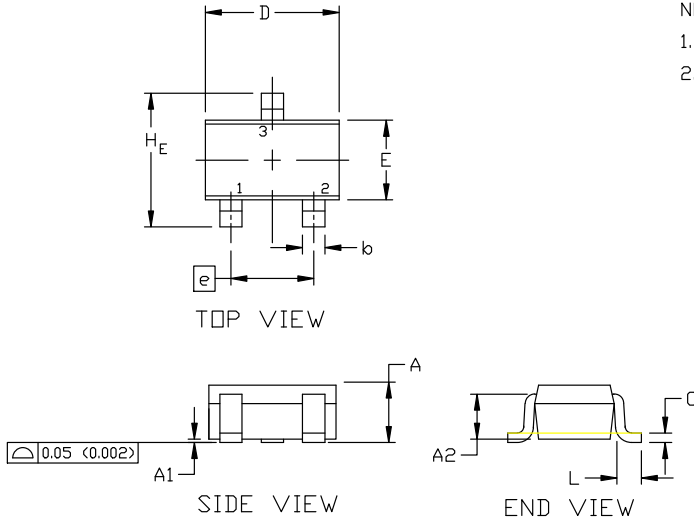
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

## SC-70 (SOT-323) CASE 419 ISSUE R

DATE 11 OCT 2022

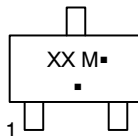


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

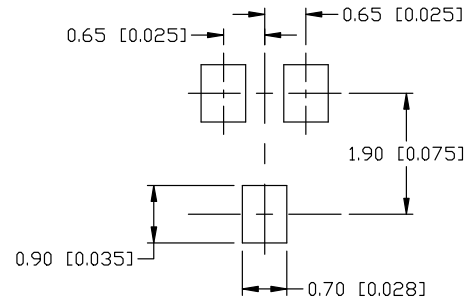
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H <sub>E</sub>	2.00	2.10	2.40	0.079	0.083	0.095

### GENERIC MARKING DIAGRAM



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### SOLDERING FOOTPRINT

- |   |   |   |  |   |   |
|---|---|---|--|---|---|
| STYLE 1:<br>CANCELLED                                 | STYLE 2:<br>PIN 1. ANODE<br>2. N.C.<br>3. CATHODE     | STYLE 3:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 4:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 5:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE          |   |
| STYLE 6:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR | STYLE 7:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 8:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN      | STYLE 9:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. ANODE-CATHODE | STYLE 11:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE |

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<b>DESCRIPTION:</b>	<b>SC-70 (SOT-323)</b>	<b>PAGE 1 OF 1</b>

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