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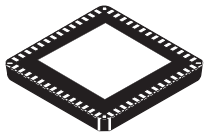
Three phase field effect transistor pre-driver

33GD3000

THREE PHASE PRE-DRIVER



EP SUFFIX (Pb-FREE)
98ASA00654D
56-PIN QFN

The 33GD3000 is a field effect transistor (FET) pre-driver designed for three phase motor control and similar applications. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

The IC contains three high-side FET pre-drivers and three low-side FET pre-drivers. Three external bootstrap capacitors provide gate charge to the high-side FETs.

The IC interfaces to a MCU via six direct input control signals, an SPI port for device setup and asynchronous reset, enable and interrupt signals. Both 5.0 V and 3.0 V logic level inputs are accepted and 5.0 V logic level outputs are provided. The integrated circuit (IC) uses SMARTMOS technology.

Features

- Fully specified from 8.0 V to 40 V covers 12 V and 24 V automotive systems
- Extended operating range from 6.0 V to 60 V covers 12 V and 48 V systems
- Gate drive capability of 1.0 A to 2.5 A
- Protection against reverse charge injection from CGD and CGS of external FETs
- Includes a charge pump to support full FET drive at low battery voltages
- Dead time is programmable via the SPI port
- Simultaneous output capability enabled via safe SPI command
- AEC-Q100 grade 1 qualified

Applications

Automotive systems

- Electro-hydraulic and electric power steering
- Braking pump
- Engine and transmission control
- Belt Starter Generator
- Turbo pump
- Actuator control
- Motor control

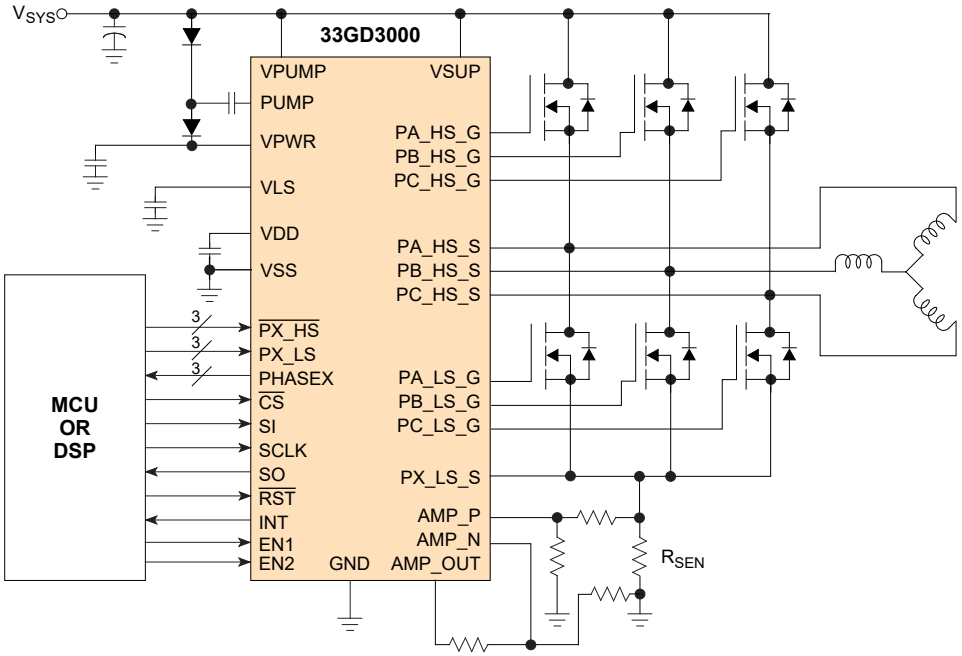


Figure 1. 33GD3000 simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package
MC33GD3000EP(1)	-40 °C to 125 °C	56-pin QFN

Notes
1. To order parts in tape and reel, add the R2 suffix to the part number.

2 Internal block diagram

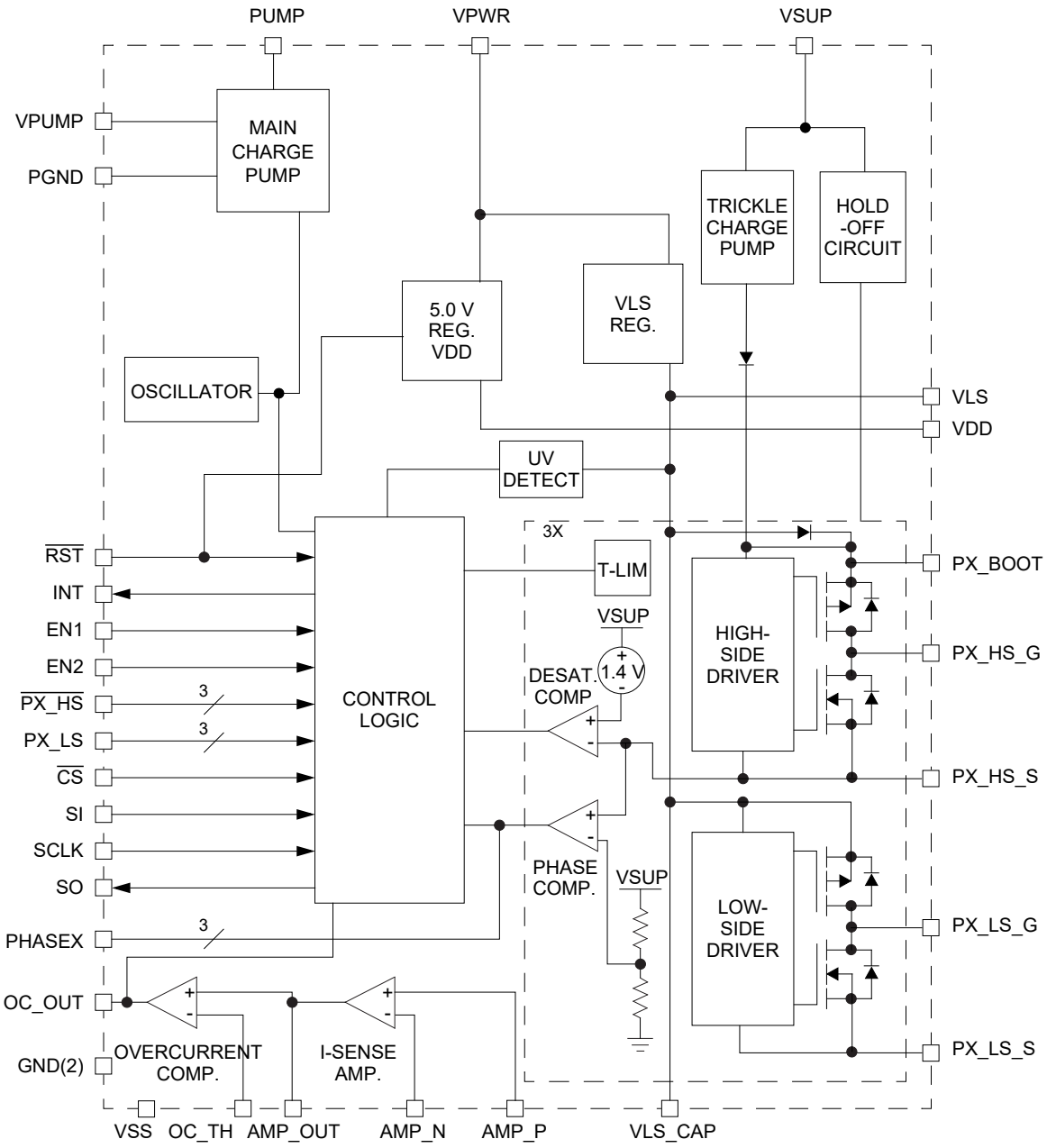


Figure 2. 33GD3000 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

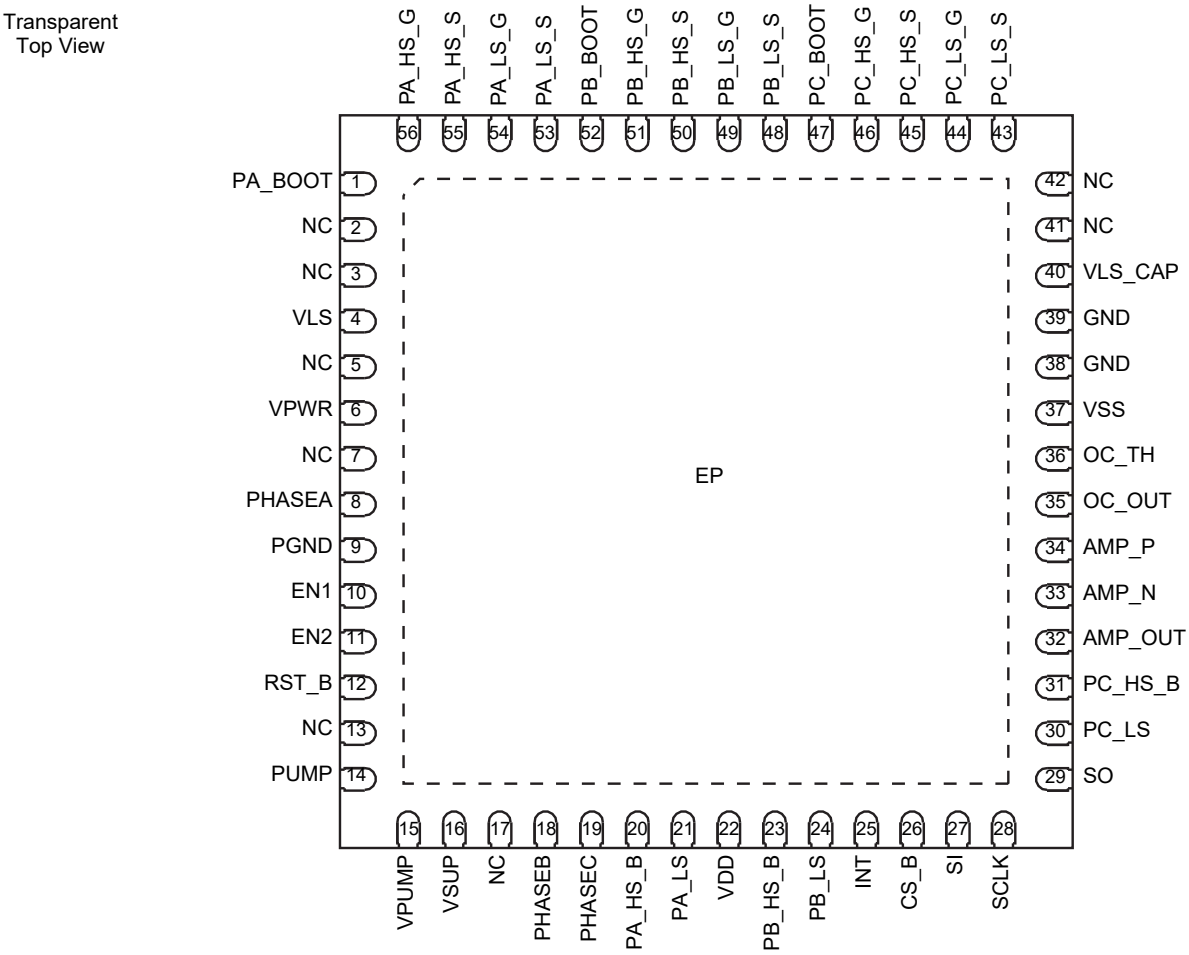


Figure 3. 33GD3000 pin connections

A functional description of each pin can be found in the Functional pin description section beginning on page 21.

Table 2. 33GD3000 pin definitions

Pin	Pin name	Pin function	Formal name	Definition
1	PA_BOOT	Analog input	Phase A bootstrap	Bootstrap capacitor for Phase A
2, 3, 5, 7, 13, 17, 41, 42	NC	No connect		No connection
4	VLS	Analog output	VLS regulator	VLS regulator output; power supply for the gate drives
6	VPWR	Power input	Voltage power	Power supply input for gate drives
8	PHASEA	Digital output	Phase A	Totem pole output of Phase A comparator; this output is low when the voltage on PA_HS_S (source of high-side FET) is less than 50% of V_{SUP}
9	PGND	Ground	Power ground	Power ground for charge pump

Table 2. 33GD3000 pin definitions

Pin	Pin name	Pin function	Formal name	Definition
10	EN1	Digital input	Enable 1	Logic signal input must be high (ANDed with EN2) to enable any gate drive output.
11	EN2	Digital input	Enable 2	Logic signal input must be high (ANDed with EN1) to enable any gate drive output
12	RST_B	Digital input	Reset	Reset input
14	PUMP	Power drive out	Pump	Charge pump output
15	VPUMP	Power input	Voltage pump	Charge pump supply
16	VSUP	Analog input	Supply voltage	Supply voltage to the load. This pin is to be connected to the common drains of the external high-side FETs
18	PHASEB	Digital output	Phase B	Totem pole output of Phase B comparator. This output is low when the voltage on PB_HS_S (source of high-side FET) is less than 50% of V_{SUP}
19	PHASEC	Digital output	Phase C	Totem pole output of Phase C comparator. This output is low when the voltage on PC_HS_S (source of high-side FET) is less than 50% of V_{SUP}
20	PA_HS_B	Digital input	Phase A high-side	Active low input logic signal enables the high-side driver for Phase A
21	PA_LS	Digital input	Phase A low-side	Active high input logic signal enables the low-side driver for Phase A
22	VDD	Analog output	VDD regulator	VDD regulator output capacitor connection
23	PB_HS_B	Digital input	Phase B high-side	Active low input logic signal enables the high-side driver for Phase B
24	PB_LS	Digital input	Phase B low-side	Active high input logic signal enables the low-side driver for Phase B
25	INT	Digital output	Interrupt	Interrupt pin output
26	CS_B	Digital input	Chip select	Chip select input. It frames SPI commands and enables SPI port.
27	SI	Digital input	Serial in	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
28	SCLK	Digital input	Serial clock	Clock for SPI port and typically is 3.0 MHz
29	SO	Digital output	Serial out	Output data for SPI port. Tri-state until CS becomes low.
30	PC_LS	Digital input	Phase C low-side	Active high input logic signal enables the low-side driver for Phase C
31	PC_HS_B	Digital input	Phase C high-side	Active low input logic signal enables the high-side driver for Phase C
32	AMP_OUT	Analog output	Amplifier output	Output of the current-sensing amplifier
33	AMP_N	Analog input	Amplifier invert	Inverting input of the current-sensing amplifier
34	AMP_P	Analog input	Amplifier non-invert	Non-inverting input of the current-sensing amplifier
35	OC_OUT	Digital output	Overcurrent out	Totem pole digital output of the overcurrent comparator
36	OC_TH	Analog input	Overcurrent threshold	Threshold of the overcurrent detector
37	VSS	Ground	Voltage source supply	Ground reference for logic interface and power supplies
38, 39	GND	Ground	Ground	Substrate and ESD reference, connect to VSS
40	VLS_CAP	Analog output	VLS regulator output capacitor	VLS regulator connection for additional output capacitor, providing low impedance supply source for low-side gate drive
43	PC_LS_S	Power input	Phase C low-side source	Source connection for Phase C low-side FET
44	PC_LS_G	Power output	Phase C low-side gate drive	Gate drive output for Phase C low-side

Table 2. 33GD3000 pin definitions

Pin	Pin name	Pin function	Formal name	Definition
45	PC_HS_S	Power input	Phase C high-side source	Source connection for Phase C high-side FET
46	PC_HS_G	Power output	Phase C high-side gate drive	Gate drive for output Phase C high-side FET
47	PC_BOOT	Analog input	Phase C bootstrap	Bootstrap capacitor for Phase C
48	PB_LS_S	Power input	Phase B low-side source	Source connection for Phase B low-side FET
49	PB_LS_G	Power output	Phase B low-side gate drive	Gate drive for output Phase B low-side
50	PB_HS_S	Power input	Phase B high-side source	Source connection for Phase B high-side FET
51	PB_HS_G	Power output	Phase B high-side gate drive	Gate drive for output Phase B high-side
52	PB_BOOT	Analog input	Phase B bootstrap	Bootstrap capacitor for Phase B
53	PA_LS_S	Power input	Phase A low-side source	Source connection for Phase A low-side FET
54	PA_LS_G	Power output	Phase A low-side gate drive	Gate drive for output Phase A low-side
55	PA_HS_S	Power input	Phase A high-side source	Source connection for Phase A high-side FET
56	PA_HS_G	Power output	Phase A high-side gate drive	Gate drive for output Phase A high-side
	EP	Ground	Exposed pad	Device performs as specified with the exposed pad un-terminated (floating) however, it is recommended the exposed pad be terminated to pin 29 (VSS) and system ground

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
ELECTRICAL RATINGS				
V_{SUP}	VSUP supply voltage • Normal operation (steady-state) • Transient survival[2]	 60 -1.5 to 80	V	(2)
V_{PWR}	VPWR supply voltage • Normal operation (steady-state) • Transient survival	 58 -1.5 to 80	V	(2)
V_{PUMP}	Charge pump (PUMP, VPUMP)	-0.3 to 40	V	
V_{LS}	VLS regulator outputs (VLS, VLS_CAP)	-0.3 to 18	V	
V_{DD}	Logic supply voltage	-0.3 to 7.0	V	
V_{OUT}	Logic output (INT, SO, PHASEA, PHASEB, PHASEC, OC_OUT)	-0.3 to 7.0	V	(3)
V_{IN}	Logic input pin voltage (EN1, EN2, $\overline{Px\_HS}$, Px_LS, SI, SCLK, $\overline{CS}$, $\overline{RST}$) 10 mA	-0.3 to 7.0	V	
V_{IN_A}	Amplifier input voltage • (Both inputs-GND), (AMP_P - GND) or (AMP_N - GND) 6.0 mA source or sink	-7.0 to 7.0	V	
V_{OC}	Overcurrent comparator threshold 10 mA	-0.3 to 7.0	V	
V_{BOOT} V_{HS_G} V_{LS_G}	Driver output voltage • High-side bootstrap (PA_BOOT, PB_BOOT, PC_BOOT) • High-side (PA_HS_G, PB_HS_G, PC_HS_G) • Low-side (PA_LS_G, PB_LS_G, PC_LS_G)	 75 75 16	V	(4)
V_{HS_G} V_{HS_S} V_{LS_G} V_{LS_S}	Driver voltage transient survival • High-side (PA_HS_G, PB_HS_G, PC_HS_G, PA_HS_S, PB_HS_S, PC_HS_S) • Low-side (PA_LS_G, PB_LS_G, PC_LS_G, PA_LS_S, PB_LS_S, PC_LS_S)	 -7.0 to 75.0 -7.0 to 75.0 -7.0 to 18.0 -7.0 to 7.0	V	(5)
V_{ESD}	ESD voltage • Human Body Model - HBM (All pins except for the pins listed below) Pins: PA_Boot, PA_HS_S, PA_HS_G, PB_Boot, PB_HS_S, PB_HS_G, PC_Boot, PC_HS_S, PC_HS_G, VPWR • Charge Device Model - CDM • Corner pins • All other pins	 ±2000 ±1000 ±300 ±250	V	(6)

Notes

2. The device can withstand load dump transient as defined by ISO 7637 with peak voltage of 80 V.
3. Short-circuit proof, the device is not damaged or induce unexpected behavior due to shorts to external sources within this range.
4. This voltage should not be applied without taking voltage at HS_S and voltage at PX_LS_S into account.
5. Actual operational limitations may differ from survivability limits. The V_{LS} - V_{LS_S} differential and the V_{BOOT} - V_{HS_S} differential must be greater than 3.0 V to ensure the output gate drive maintains a commanded OFF condition on the output.
6. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).

Table 3. Maximum ratings (continued)

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
THERMAL RATINGS				
T_{STG}	Storage temperature	-55 to +150	°C	
T_J	Operating junction temperature	-40 to +150	°C	
$R_{\theta JC}$	Thermal resistance • Junction-to-Case	1.5	°C/W	(7)
T_{SOLDER}	Soldering temperature	Note 9	°C	(8)

Notes

7. Case is considered EP - pin 55 under the body of the device. The actual power dissipation of the device is dependent on the operating mode, the heat transfer characteristics of the board and layout and the operating voltage. See Figure 23 and Figure 24 for examples of power dissipation profiles of two common configurations. Operation above the maximum operating junction temperature results in a reduction in reliability leading to malfunction or permanent damage to the device.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes and enter the core ID) to view all orderable parts, and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
POWER INPUTS						
V_{PWR_ST}	VPWR supply voltage startup threshold	–	6.0	8.0	V	(10)
I_{SUP}	VSUP supply current, V_{PWR} = V_{SUP} = 40 V $\overline{RST}$ and ENABLE = 5.0 V • No output loads on gate drive pins, no PWM • No output loads on gate drive pins, 20 kHz, 50% duty cycle	 – –	 1.0 –	 – 10	mA	
I_{PWR_ON}	VPWR supply current, V_{PWR} = V_{SUP} = 40 V $\overline{RST}$ and ENABLE = 5.0 V • No output loads on gate drive pins, no PWM, outputs initialized • Output loads = 620 nC per FET, 20 kHz PWM	 – –	 11 –	 20 95	mA	 (11)
I_{SUP} I_{PWR}	Sleep state supply current, $\overline{RST}$ = 0 V • V_{SUP} = 40 V • V_{PWR} = 40 V	 – –	 14 56	 30 100	 µA	
V_{GATESS}	Sleep state output gate voltage • IG < 100 µA	–	–	1.3	V	
V_{BOOT}	Trickle charge pump (bootstrap voltage, V_{SUP} = 14 V	22	28	32	V	(12)
V_F	Bootstrap diode forward voltage at 10 mA	–	–	1.2	V	
VDD INTERNAL REGULATOR						
V_{DD}	V_{DD} output voltage, V_{PWR} = 8.0 V to 40 V, C = 0.47 µF • External load I_{DD_EXT} = 0 mA to 1.0 mA	4.5	–	5.5	V	(13)
I_{DD}	Internal V_{DD} supply current, V_{DD} = 5.5 V, no external load	–	–	12	mA	
VLS REGULATOR						
I_{PEAK}	Peak output current, V_{PWR} = 16 V, V_{LS} = 10 V	350	600	800	mA	
V_{LS}	Linear regulator output voltage, I_{VLS} = 0 mA to 60 mA, V_{PWR} > V_{LS} + 2.0 V	13.5	15	17	V	(14)
V_{THVLS}	VLS disable threshold	7.5	8.0	8.5	V	(15)

Notes

10. Operation with the Charge Pump is recommended when minimum system voltage could be less than 14 V. V_{PWR} must exceed this threshold in order for the Charge Pump and V_{DD} regulator to startup and drive V_{PWR} to > 8.0 V. Once V_{PWR} exceeds 8.0 V, the circuits continue to operate even if system voltage drops below 6.0 V.
11. This parameter is guaranteed by design. It is not production tested.
12. See Figure 11 for typical capability to maintain gate voltage with a 5.0 µA load.
13. Minimum external capacitor for stable V_{DD} operation is 0.47 µF.
14. Recommended external capacitor for the V_{LS} regulator is 2.2 µF low ESR at each pin VLS and VLS_CAP.
15. When V_{LS} is less than this value, the outputs are disabled and HOLDOFF circuits are active. Recovery requires initialization when V_{LS} rises above this threshold again. A filter delay of approximately 700 ns on the comparator output eliminates responses to spurious transients on V_{LS}.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
CHARGE PUMP						
$R_{DS(ON)\_HS}$ $R_{DS(ON)\_LS}$ V_{THREG}	Charge pump • High-side switch on resistance • Low-side switch on resistance • Regulation threshold difference	 – – 250	 6.0 5.0 500	 10 9.4 900	 Ω Ω mV	(16), (17)
V_{CP}	Charge pump output voltage • I_{OUT} = 40 mA, 6.0 V < V_{SYS} < 8.0 V • I_{OUT} = 40 mA, V_{SYS} > = 8.0 V	 8.5 12	 9.5 –	 – –	 V	(17), (18)
GATE DRIVE						
$R_{DS(ON)\_H\_SRC}$	High-side driver on resistance (sourcing) • V_{PWR} = V_{SUP} = 16 V, -40 °C ≤ T_A ≤ 25 °C • V_{PWR} = V_{SUP} = 16 V, 25 °C < T_A ≤ 125 °C	 – –	 – –	 6.0 8.5	 Ω	
$R_{DS(ON)\_H\_SINK}$	High-side driver on resistance (sinking) • V_{PWR} = V_{SUP} = 16 V	–	–	3.0	Ω	
I_{HS_INJ}	High-side current injection allowed without malfunction	–	–	0.5	A	(17), (19)
$R_{DS(ON)\_L\_SRC}$	Low-side driver on resistance (sourcing) • V_{PWR} = V_{SUP} = 16 V, -40 °C ≤ T_A ≤ 25 °C • V_{PWR} = V_{SUP} = 16 V, 25 °C < T_A ≤ 125 °C	 – –	 – –	 6.0 8.5	 Ω	
$R_{DS(ON)\_L\_SINK}$	Low-side driver on-resistance (sinking) • V_{PWR} = V_{SUP} = 16 V	–	–	3.0	Ω	
I_{LS_INJ}	Low-side current injection allowed without malfunction	–	–	0.5	A	(17), (19)
V_{GS_H} V_{GS_L}	Gate source voltage, V_{PWR} = V_{SUP} = 40 V • High-side, I_{GATE} = 0 • Low-side, I_{GATE} = 0	 13 13	 14.8 15.4	 16.5 17	 V	(20)
$V_{HS\_G\_HOLD}$	Reverse high-side gate holding voltage • Gate output holding current = 2.0 µA • Gate output holding current = 5.0 µA, V_{SUP}<26 V • Gate output holding current = 5.0 µA, V_{SUP}<40 V	 – – –	 10 10 –	 15 15 15	 V	(21)

Notes

16. When VLS is this amount below the normal VLS linear regulation threshold, the charge pump is enabled.
17. This parameter is a design characteristic, not production tested.
18. V_{SYS} is the system voltage on the input to the charge pump. Recommended external components: 1.0 µF MLC, MUR 120 diode.
19. Current injection only occurs during output switch transitions. The IC is immune to specified injected currents for a duration of approximately 1.0 µs after an output switch transition. 1.0 µs is sufficient for all intended applications of this IC.
20. If a slightly higher gate voltage is required, larger bootstrap capacitors are required. At high duty cycles, the bootstrap voltage may not recover completely, leading to a higher output on-resistance. This effect can be minimized by using low ESR capacitors for the bootstrap and the VLS capacitors.
21. High-side gate holding voltage is the voltage between the gate and source of the high-side FET when held in an on condition. The trickle charge pump supplies bias and holding current for the high-side FET gate driver and output to maintain voltages after bootstrap events. See Figure 11 for typical 100% high-side gate voltage with a 5.0 µA load. This parameter is a design characteristic, not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
OVERCURRENT COMPARATOR						
V_{CM}	Common mode input range	2.0	–	V_{DD}-0.02	V	(22)
V_{OS_OC}	Input offset voltage	-50	–	50	mV	
V_{OC_HYST}	Overcurrent comparator threshold hysteresis	50		300	mV	(23)
V_{OH} V_{OL}	Output voltage • High level at I_{OH} = -500 µA • Low level at I_{OL} = 500 µA	0.85 V_{DD} –	– –	V_{DD} 0.5	V	
HOLD OFF CIRCUIT						
I_{HOLD}	Hold off current (at each GATE pin) • 3.0 V < V_{SUP} < 40 V, V_{GATE} = 1.0 V	10	–	300	µA	(24)
PHASE COMPARATOR						
V_{IH_TH}	High level input voltage threshold	0.5 V_{SUP}	–	0.65 V_{SUP}	V	
V_{IL_TH}	Low level input voltage threshold	0.3 V_{SUP}	–	0.45 V_{SUP}	V	
V_{OH}	High level output voltage at I_{OH} = -500 µA	0.85 V_{DD}	–	V_{DD}	V	
V_{OL}	Low level output voltage at I_{OL} = 500 µA	–	–	0.5	V	
R_{IN}	High-side source input resistance	–	40	–	kΩ	(23), (25)
DESATURATION DETECTOR						
V_{DES_TH}	Desaturation detector threshold	1.2	1.4	1.6	V	(26)
CURRENT SENSE AMPLIFIER						
R_S	Recommended external series resistor (see Figure 9)	–	1.0	–	kΩ	
R_{FB}	Recommended external feedback resistor (see Figure 9) • Limited by the output voltage dynamic range	5.0	–	15	kΩ	(27)
V_{ID}	Maximum input differential voltage (see Figure 9) • V_{ID} = V_{AMP_P} - V_{AMP_N}	-800	–	+800	mV	
V_{CM}	Input common mode range	-0.5	–	3.0	V	(23), (28)
V_{OS}	Input offset voltage • R_S = 1.0 kΩ, V_{CM} = 0.0 V	-15	–	+15	mV	
$\delta V_{OS}/\delta T$	Input offset voltage drift	–	-10	–	µV/°C	(23)
I_B	Input bias current • V_{CM} = 2.0 V	-200	–	+200	nA	

Notes

22. As long as one input is in the common mode range there is no phase inversion on the output.
23. This parameter is a design characteristic, not production tested.
24. The hold off circuit is designed to operate over the full operating range of V_{SUP}. The specification indicates the conditions used in production test. Hold off is activated at V_{POR} or V_{THVLS}.
25. Input resistance is impedance from the high-side source and is referenced to V_{SS}. Approximate tolerance is ±20%.
26. Desaturation is measured as the voltage drop below V_{SUP}, thus the threshold is compared to the drain-source voltage of the external high-side FET. See Figure 5.
27. The current sense amplifier is unity gain stable with a phase margin of approximately 45°. See Figure 10.
28. As long as one input is within V_{CM} the output is guaranteed to have the correct phase. Exceeding the common mode rails on one input does not cause a phase inversion on the output.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
CURRENT SENSE AMPLIFIER (CONTINUED)						
I_{OS}	Input offset current • I_{OS} = I_{AMP_P} - I_{AMP_N}	-80	–	+80	nA	
$\delta I_{OS}/\delta T$	Input offset current drift	–	40	–	pA/°C	(29)
V_{OH} V_{OL}	Output voltage • High level with R_{LOAD} = 10 kΩ to V_{SS} • Low level with R_{LOAD} = 10 kΩ to V_{DD}	V_{DD}-0.2 –	– –	V_{DD} 0.2	V	
R_I	Differential input resistance	1.0	–	–	MΩ	
I_{SC}	Output short-circuit current	5.0	–	–	mA	
C_I	Common mode input capacitance at 10 kHz	–	–	10	pF	(29), (30)
C_{MRR}	Common mode rejection ratio at DC • CMRR = 20*Log ((V_{OUT_DIFF}/V_{IN_DIFF}) * (V_{IN_CM}/V_{OUT_CM}))	60	80	–	dB	
A_{OL}	Large signal open loop voltage gain (DC)	–	78	–	dB	(29), (30)
NL	Nonlinearity • RL = 1.0 kΩ, C_L = 500 pF, 0.3 < V_O < 4.8 V, Gain = 5.0 to 15	-1.0	–	+1.0	%	(29), (30)
SUPERVISORY AND CONTROL CIRCUITS						
V_{IH} V_{IL}	Logic inputs (Px_LS, $\overline{Px\_HS}$, EN1, EN2) • High level input voltage threshold • Low level input voltage threshold	2.1 –	– –	– 0.9	V	(31)
V_{IH} V_{IL}	Logic inputs (SI, SCLK, $\overline{CS}$) • High level input voltage threshold • Low level input voltage threshold	2.1 –	– –	– 0.9	V	(31), (32)
V_{IHYS}	Input logic threshold hysteresis • Inputs Px_LS, SI, SCLK, $\overline{CS}$, $\overline{Px\_HS}$, EN1, EN2	100	250	450	mV	(32)
I_{INPD}	Input pull-down current, (Px_LS, SI, SCLK, EN1, EN2) • 0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}	8.0	–	18	µA	
I_{INPU}	Input pull-up current, ($\overline{CS}$, $\overline{Px\_HS}$) • 0 ≤ V_{IN} ≤ 0.7 V_{DD}	10	–	25	µA	(33)
C_{IN}	Input capacitance • 0.0 V ≤ V_{IN} ≤ 5.5 V	–	15	–	pF	(32)
$V_{TH\_\overline{RST}}$	$\overline{RST}$ threshold	1.0	–	2.1	V	(34)
$R_{\overline{RST}}$	$\overline{RST}$ pull-down resistance • 0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}	40	60	85	kΩ	
V_{POR}	Power-OFF $\overline{RST}$ threshold, (V_{DD} falling)	3.4	4.0	4.5	V	
V_{SOH}	SO high level output voltage • I_{OH} = 1.0 mA	0.9 V_{DD}	–	–	V	
V_{SOL}	SO low level output voltage • I_{OL} = 1.0 mA	–	–	0.1 V_{DD}	V	

Notes

29. This parameter is a design characteristic, not production tested.
30. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.
31. Logic threshold voltages derived relative to a 3.3 V 10% system.
32. This parameter is guaranteed by design, not production tested.
33. Pull-up circuits do not allow back biasing of V_{DD}.
34. There are two elements in the $\overline{RST}$ circuit: 1) one generally lower threshold enables the internal regulator; 2) the second removes the reset from the internal logic.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SUPERVISORY AND CONTROL CIRCUITS						
$I_{SO\_LEAK\_T}$	SO tri-state leakage current • $\overline{CS}$ = 0.7 V_{DD}, 0.3 V_{DD} ≤ V_{SO} ≤ 0.7 V_{DD}	-1.0	–	1.0	µA	
C_{SO_T}	SO tri-state capacitance (35), (36) • 0.0 V ≤ V_{IN} ≤ 5.5 V	–	15	–	pF	
V_{OH}	INT high level output voltage • I_{OH} = -500 µA	0.85 V_{DD}	–	V_{DD}	V	
V_{OL}	INT low level output voltage • I_{OL} = 500 µA	–	–	0.5	V	
THERMAL WARNING						
T_{WARN}	Thermal warning temperature (35), (37)	150	170	185	°C	
T_{HYST}	Thermal hysteresis (35)	8.0	10	12	°C	

Notes

35. This parameter is guaranteed by design, not production tested.
36. This parameter applies to the OFF state (tri-stated) condition of SO is guaranteed by design but is not production tested.
37. The Thermal Warning circuit does not force IC shutdown above this temperature. It is possible to set a bit in the MASK register to generate an interrupt when overtemperature is detected, and the status bit always indicates if any of the three individual Thermal Warning circuits in the IC sense a fault.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
INTERNAL REGULATORS						
t_{PU_VDD}	V_{DD} power-up time (Until INT High) • 8.0 V ≤ V_{PWR}	–	–	2.0	ms	(38), (39)
t_{PU_VLS}	VLS power-up time • 16 V ≤ V_{PWR}	–	–	2.0	ms	(39), (40)
CHARGE PUMP						
f_{OSC}	Charge pump oscillator frequency	90	125	190	kHz	
SR_{CP}	Charge pump slew rate	–	100	–	V/µs	(41)
GATE DRIVE						
t_{ONH}	High-side turn on time • Transition time from 1.0 V to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	–	20	35	ns	(42)
t_{D_ONH}	High-side turn on delay • Delay from command to 1.0 V, (Figure 7)	130	265	386	ns	(43)
t_{OFFH}	High-side turn off time • Transition time from 10 V to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	–	20	35	ns	(42)
t_{D_OFFH}	High-side turn off delay • Delay from command to 10 V, (Figure 8)	130	265	386	ns	(43)
t_{ONL}	Low-side turn on time • Transition time from 1.0 V to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	–	20	35	ns	(42)
t_{D_ONL}	Low-side turn on delay • Delay from command to 1.0 V, (Figure 7)	130	265	386	ns	(43)
t_{OFFL}	Low-side turn off time • Transition time from 10 V to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	–	20	35	ns	(42)
t_{D_OFFL}	Low-side turn off delay • Delay from command to 10 V, (Figure 8)	130	265	386	ns	(43)
t_{D_DIFF}	Same phase command delay match	-20	0.0	+20	ns	(44)
t_{DUR}	Thermal filter duration	8.0	–	30	µs	(45)

Notes

38. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitor on V_{DD}.
39. This specification is based on capacitance of 0.47 µF on VDD, 2.2 µF on VLS and 2.2 µF on VLS_CAP.
40. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitors on VLS and VLS_CAP. This delay includes the expected time for V_{DD} to rise.
41. The charge pump operating at 12 V V_{SYS}, 1.0 µF pump capacitor, MUR120 diodes and 47 µF filter capacitor.
42. This parameter is guaranteed by characterization, not production tested.
43. These delays include all logic delays except deadtime. All internal logic is synchronous with the internal clock. The total delay includes one clock period for state machine decision block, an additional clock period for FULLON mux logic, input synchronization time and output driver propagation delay. Subtract one clock period for operation in FULLON mode which bypasses the state machine decision block. Synchronization time accounts for up to one clock period of variation. See Figure 6.
44. The maximum separation or overlap of the high and low-side gate drives, due to propagation delays when commanding one ON and the other OFF simultaneously, is guaranteed by design.
45. The output of the overtemperature comparator goes through a digital filter before generating a warning or interrupt.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
GATE DRIVE (CONTINUED)						
t_{DC}	Duty cycle	0.0	–	96	%	(46), (47)
t_{DC}	100% duty cycle duration	–	–	Unlimited	s	(46), (47)
t_{MAX}	Maximum programmable deadtime	10.2	15	19.6	µs	(48)
OVERCURRENT COMPARATOR						
t_{OC}	Overcurrent protection filter time	0.9	–	3.5	µs	
t_{ROC}	Rise time (OC_OUT) • 10% - 90%, C_L = 100 pF	10	–	240	ns	
t_{FOC}	Fall time (OC_OUT) • 90% - 10%, C_L = 100 pF	10	–	200	ns	
DESATURATION DETECTOR AND PHASE COMPARATOR						
	Phase comparator propagation delay time to 50% of V_{DD}; C_L ≤ 100 pF					
t_R	• Rising edge delay	–	–	200	ns	
t_F	• Falling edge delay	–	–	350		
t_{MATCH}	Phase comparator match (prop delay mismatch of three phases) • C_L = 100 pF	–	–	100	ns	(46)
t_{BLANK}	Desaturation and phase error blanking time	4.7	7.1	9.1	µs	(49)
t_{FILT}	Desaturation filter time (Filter time is digital) • Fault must be present for this time to trigger	640	937	1231	ns	(46)
CURRENT SENSE AMPLIFIER						
t_{SETTLE}	Output settle time to 99% • RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5 to 15	–	1.0	2.0	µs	(46), (50)
t_{IS_RISE}	Output rise time to 90% • RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5.0 to 15	–	–	1.0	µs	(51)
t_{IS_FALL}	Output fall time to 10% • RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5.0 to 15	–	–	1.0	µs	(51)
SR_5	Slew rate at gain = 5.0 • RL = 1.0 kΩ, C_L = 20 pF	5.0	–	–	V/µs	(46)
f_M	Phase margin at gain = 5.0	–	30	–	°	(46)

Notes

46. This parameter is guaranteed by design, not production tested.
47. As duty cycle approaches the limit of 100% or 0% there is a maximum and minimum which is not achievable due to deadtime, propagation delays, switching times and charge time of the bootstrap capacitor (for the high-side FET). 0% is available by definition (FET always OFF) and unlimited ON (100%) is possible as long as gate charge maintenance current is within the trickle charge pump capacity.
48. A minimum deadtime of 0.0 can be set via an SPI command. When deadtime is set via a DEADTIME command, a minimum of 1 clock cycle duration and a maximum of 255 clock cycles is set using the internal time base clock as a reference. Commands exceeding this value limits at this value.
49. Blanking time, t_{BLANK}, is applied to all phases simultaneously when switching ON any output FET. This precludes false errors due to system noise during the switching event.
50. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.
51. Rise and fall times are measured from the transition of a step function on the input to 90% of the change in output voltage.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
CURRENT SENSE AMPLIFIER (CONTINUED)						
G_{BW}	Unity gain bandwidth • RL = 1.0 kΩ, C_L = 100 pF	–	20	–	MHz	(52)
BW_G	Bandwidth at gain = 15 • R_L = 1.0 kΩ, C_L = 50 pF	2.0	–	–	MHz	(52)
CMR	Common mode rejection (CMR) with V_{IN} • V_{IN_CM} = 400 mV*sin(2*π*freq*t) • V_{IN_DIF} = 0.0 V, RS = 1.0 kΩ • R_{FB} = 15 kΩ, V_{REFIN} = 0.0 V CMR = 20*Log(V_{OUT}/V_{IN_CM}) • Freq = 100 kHz • Freq = 1.0 MHz • Freq = 10 MHz	 50 40 30	 – – –	 – – –	dB	(52)
SUPERVISORY AND CONTROL CIRCUITS						
t_{PROP}	EN1 and EN2 propagation delay	–	–	280	ns	
t_{RINT}	INT rise time CL = 100 pF	10	–	250	ns	
t_{FINT}	INT fall time CL = 100 pF	10	–	200	ns	
$t_{PROPINT}$	INT propagation time	–	–	250	ns	
t_{TRRST}	$\overline{RST}$ transition time (rise and fall)	–	–	1.25	µs	(52),(53)
SPI INTERFACE TIMING						
f_{OP}	Maximum frequency of SPI operation	–		4.0	MHz	
f_{TB}	Internal time base	13	17	25	MHz	
TC_{TB}	Internal time base drift from value at 25 °C	-5.0	–	5.0	%	(52)
t_{LEAD}	Falling edge of $\overline{CS}$ to rising edge of SCLK (required setup time)	100	–	–	ns	(52)
t_{LAG}	Falling edge of SCLK to rising edge of $\overline{CS}$ (required setup time)	100	–	–	ns	(52)
t_{SISU}	SI to falling edge of SCLK (required setup time)	25	–	–	ns	(52)
t_{SIHOLD}	Falling edge of SCLK to SI (required setup time)	25	–	–	ns	(52)
t_{RSI}	SI, $\overline{CS}$, SCLK signal rise time	–	5.0	–	ns	(52), (54)
t_{FSI}	SI, $\overline{CS}$, SCLK signal fall time	–	5.0	–	ns	(52), (54)
t_{SOEN}	Time from falling edge of $\overline{CS}$ to SO low-impedance	–	55	100	ns	(52), (55)
t_{SODIS}	Time from rising edge of $\overline{CS}$ to SO high-impedance	–	100	125	ns	(52), (56)
t_{VALID}	Time from rising edge of SCLK to SO data valid	–	80	125	ns	(52), (57)
t_{DT}	Time from rising edge of $\overline{CS}$ to falling edge of the next $\overline{CS}$	200	–	–	ns	(52)

Notes

52. This parameter is guaranteed by design, not production tested.
53. t_{TRRST} is given as a design guideline. The bounds for this specification are VPWR ≤ 58 V, total capacitance on VLS > 1.0 µF.
54. Rise and fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
55. Time required for valid output status data to be available on SO pin.
56. Time required for output states data to be terminated at SO pin.
57. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

4.4 Timing diagrams

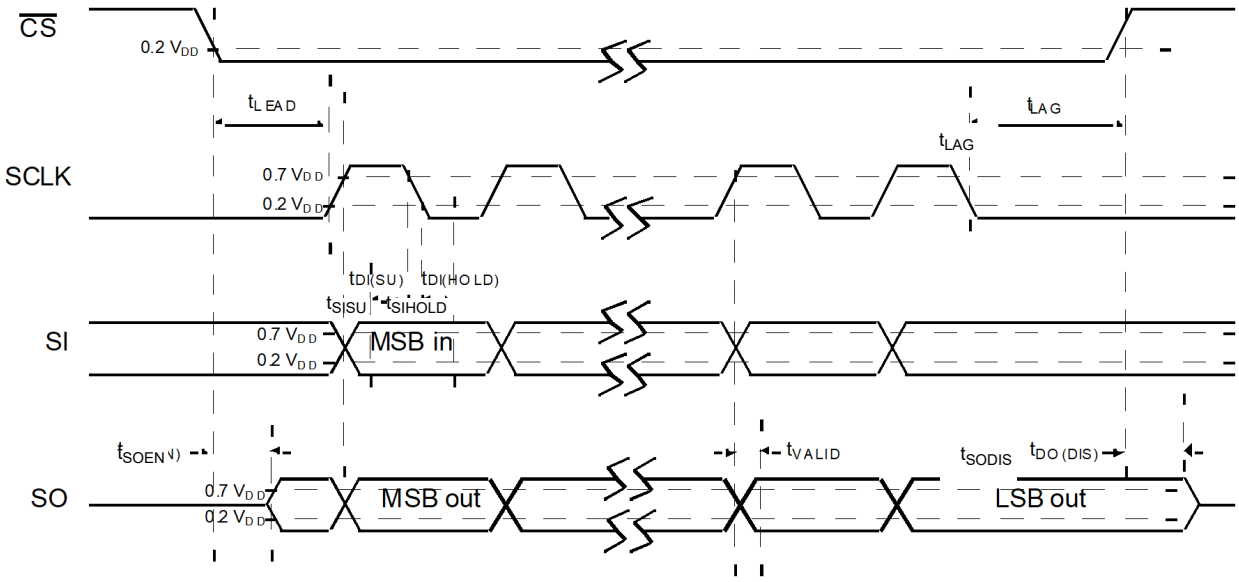


Figure 4. SPI interface timing

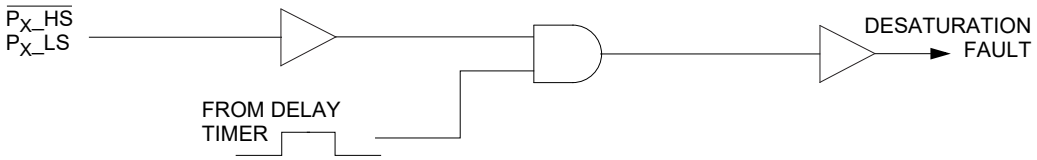


Figure 5. Desaturation blanking and filtering detail

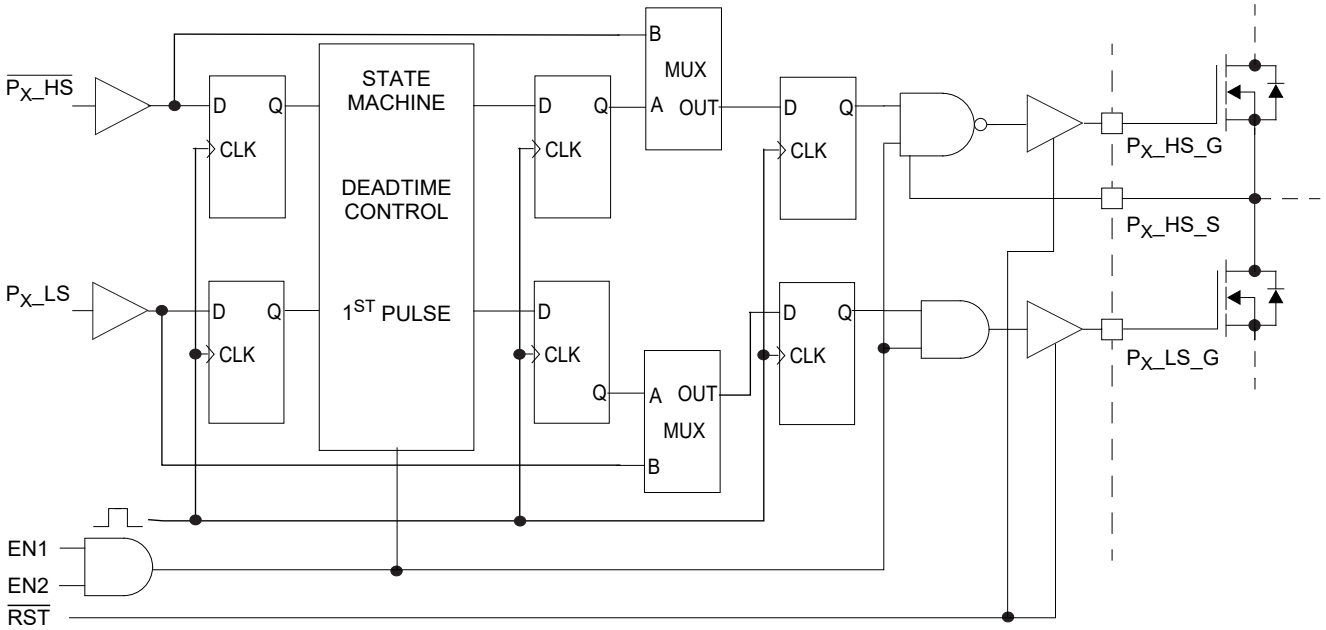


Figure 6. Deadtime control delays

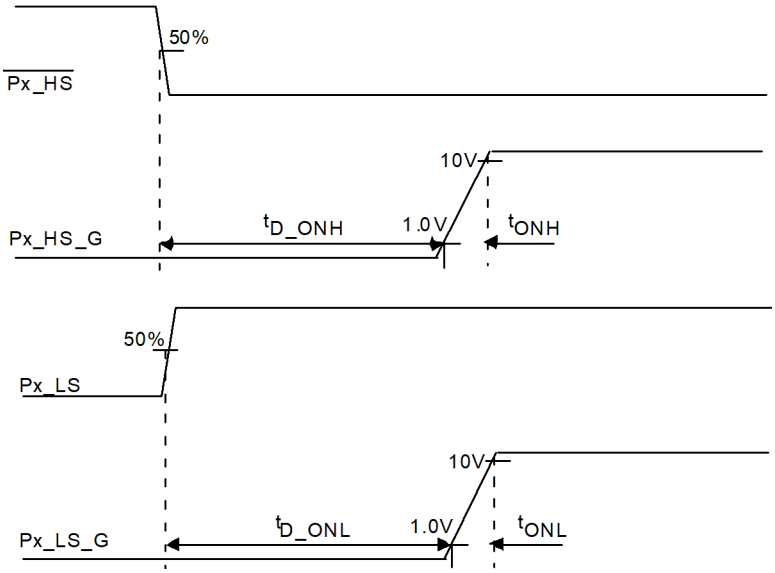


Figure 7. Driver turn-on time and turn-on delay

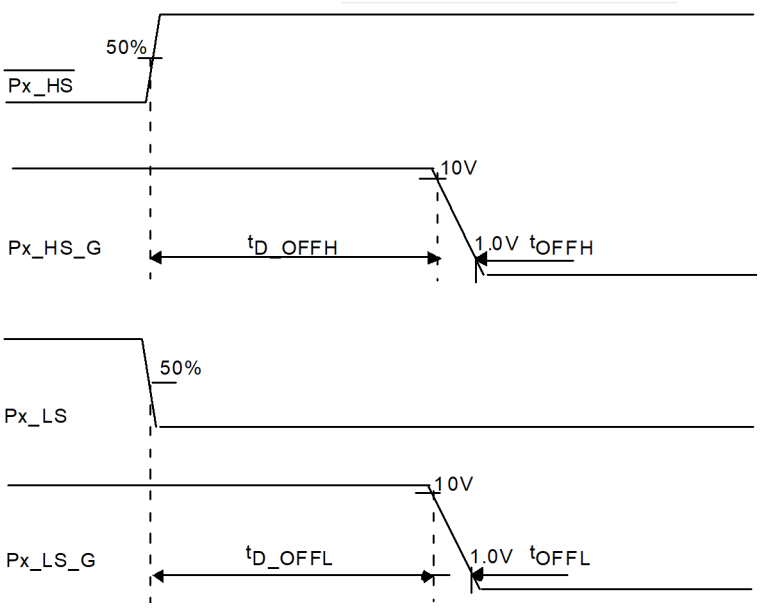


Figure 8. Driver turn-off time and turn-off delay

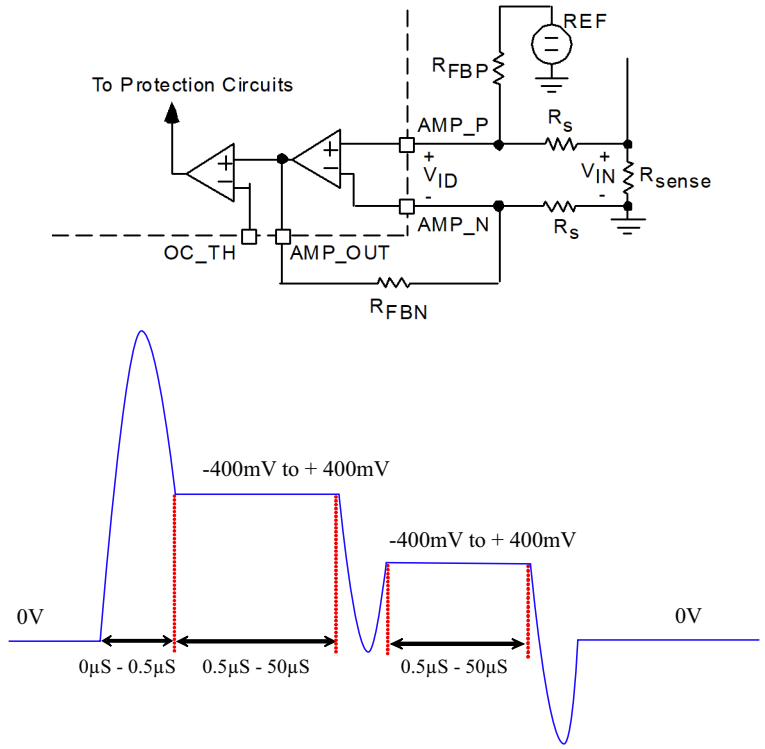


Figure 9. Current amplifier and input waveform (V_{IN} voltage across R_{SENSE})

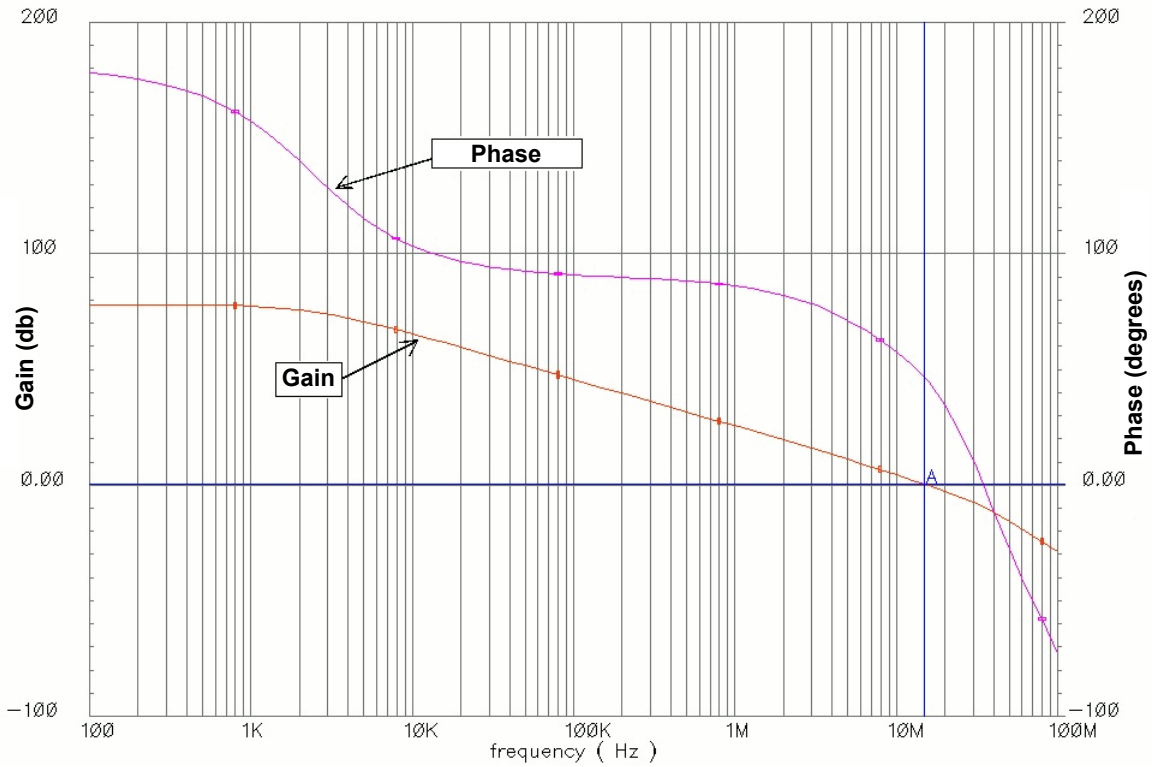


Figure 10. Typical amplifier open-loop gain and phase vs. frequency

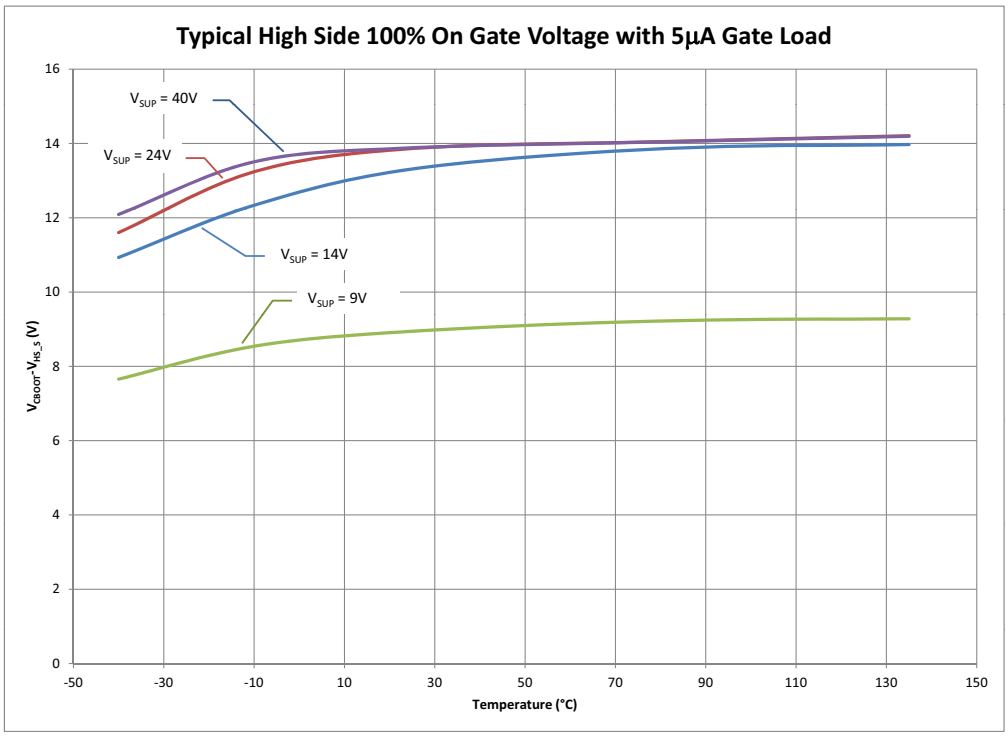


Figure 11. Typical high-side 100% on gate voltage with 5.0 µA gate load

5 Functional descriptions

5.1 Introduction

The 33GD3000 provides an interface between an MCU and the large FETs used to drive three phase loads. A typical load FET may have an on resistance of 4.0 mΩ or less and could require a gate charge of over 400 nC to fully turn on. The IC can operate in automotive 12 V to 42 V environments.

Because there are so many methods of controlling three phase systems, the IC enforces few constraints on driving the FETs. It does provide deadtime (cross-over) blanking and logic, both of which can be overridden, ensuring both FETs in a phase are not simultaneously enabled. An SPI port is used to configure the IC modes.

5.2 Functional pin description

5.2.1 Phase A (PHASEA)

This pin is the totem pole output of the Phase A comparator. This output is low when the voltage on Phase A high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP}.

5.2.2 Power Ground (PGND)

This pin is power ground for the charge pump. It should be connected to VSS, however routing to a single point ground on the PCB may help to isolate charge pump noise.

5.2.3 Enable 1 and Enable 2 (EN1, EN2)

Both of these logic signal inputs must be high to enable any gate drive output. When either or both are low, the internal logic (SPI port, etc.) still functions normally, but all gate drives are forced off (external power FET gates pulled low). The signal is asynchronous.

When EN1 and EN2 return high to enable the outputs, each LS driver must be pulsed ON before the corresponding HS driver can be commanded ON. This ensures the bootstrap capacitors are charged. See Initialization requirements on page 39.

5.2.4 Reset ($\overline{RST}$)

When the reset pin is low the integrated circuit (IC) is in a low power state. In this mode all outputs are disabled, internal bias circuits are turned off, and a small pull-down current is applied to the output gate drives. The internal logic is reset within 77 ns of RESET going low. When $\overline{RST}$ is low, the IC consumes minimal current.

5.2.5 Charge Pump Out (PUMP)

This pin is the switching node of the charge pump circuit. The output of the internal charge pump support circuit. When the charge pump is used, it is connected to the external pumping capacitor. This pin may be left floating if the charge pump is not required.

5.2.6 Charge Pump Input (VPUMP)

This pin is the input supply for the charge pump circuit. When the charge pump is required, this pin should be connected to a polarity protected supply. This input should never be connected to a supply greater than 40 V. If the charge pump is not required this pin may be left floating.

5.2.7 VSUP Input (VSUP)

The supply voltage pin should be connected to the common connection of the high-side FETs. It is the reference bias for the Phase Comparators and Desaturation Comparator. It is also used to provide power to the internal steady state trickle charge pump and to energize the hold off circuit.

5.2.8 Phase B (PHASEB)

This pin is the totem pole output of the Phase B comparator. This output is low when the voltage on Phase B high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP}.

5.2.9 Phase C (PHASEC)

This pin is the totem pole output of the Phase C comparator. This output is low when the voltage on Phase C high-side source (source of the high-side load FET) is less than 50 percent of V_{SUP}.

5.2.10 Phase A High-side Input ($\overline{\text{PA\_HS}}$)

This input logic signal pin enables the high-side driver for Phase A. The signal is active low, and is pulled up by an internal current source.

5.2.11 Phase A Low-side Input (PA_LS)

This input logic signal pin enables the low-side driver for Phase A. The signal is active high, and is pulled down by an internal current sink.

5.2.12 VDD Voltage Regulator (VDD)

VDD is an internally generated 5.0 V supply. The internal regulator provides continuous power to the IC and is a supply reference for the SPI port. A 0.47 µF (min.) decoupling capacitor must be connected to this pin. This regulator is intended for internal IC use and can supply only a small (1.0 mA) external load current.

A power-on-reset (POR) circuit monitors this pin and until the voltage rises above the threshold, the internal logic resets; driver outputs are tri-stated, and SPI communication disabled. The VDD regulator can be disabled by asserting the $\overline{\text{RST}}$ signal low. The VDD regulator is powered from the VPWR pin.

5.2.13 Phase B High-side Control Input ($\overline{\text{PB\_HS}}$)

This pin is the input logic signal, enabling the high-side driver for Phase B. The signal is active low, and is pulled up by an internal current source.

5.2.14 Phase B Low-side Input (PB_LS)

This pin is the input logic signal, enabling the low-side driver for Phase B. The signal is active high, and is pulled down by an internal current sink.

5.2.15 Interrupt (INT)

The Interrupt pin is a totem pole logic output. When a fault is detected, this pin pulls high until it is cleared by executing the Clear Interrupt command via the SPI port. The faults capable of causing an interrupt can be masked via the MASK0 and MASK1 SPI registers to customize the response.

5.2.16 Chip Select ($\overline{\text{CS}}$)

Chip select is a logic input which frames the SPI commands and enables the SPI port. This signal is active low, and is pulled up by an internal current source.

5.2.17 Serial In (SI)

The Serial In pin is used to input data to the SPI port. Clocked on the falling edge of SCLK, it is the most significant bit (MSB) first. This pin is pulled down by an internal current sink.

5.2.18 Serial Clock (SCLK)

This logic input is the clock is used for the SPI port. The SCLK typically runs at 3.0 MHz (up to 5.0 MHz) and is pulled down by an internal current sink.

5.2.19 Serial Out (SO)

Output data for the SPI port streams from this pin. It is tri-stated until $\overline{CS}$ is low. New data appears on rising edges of SCLK in preparation for latching by the falling edge of SCLK on the master.

5.2.20 Phase C Low-side Input (PC_LS)

This input logic pin enables the low-side driver for Phase C. This pin is an active high, and is pulled down by an internal current sink.

5.2.21 Phase C High-side Input ($\overline{PC\_HS}$)

This input logic pin enables the high-side driver for Phase C. This signal is active low, and is pulled up by an internal current source.

5.2.22 Amplifier Output (AMP_OUT)

This pin is the output for the current sensing amplifier. It is also the sense input to the overcurrent comparator.

5.2.23 Amplifier Inverting Input (AMP_N)

The inverting input to the current sensing amplifier.

5.2.24 Amplifier Non-Inverting Input (AMP_P)

The non-inverting input to the current sensing amplifier.

5.2.25 Overcurrent Comparator Output (OC_OUT)

The overcurrent comparator output is a totem pole logic level output. A logic high indicates an overcurrent condition.

5.2.26 Overcurrent Comparator Threshold (OC_TH)

This input sets the threshold level of the overcurrent comparator.

5.2.27 Voltage Source Supply (VSS)

VSS is the ground reference for the logic interface and power supplies.

5.2.28 Ground (GND0,GND1)

These two pins are connected internally to VSS by a 1.0 Ω resistor. They provide device substrate connections and also the primary return path for ESD protection.

5.2.29 VLS Regulator Capacitor (VLS_CAP)

This connection is for a capacitor which provides a low-impedance for switching currents on the gate drive. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents must be connected between this pin and VSS.

This is the same DC node as VLS, but it is physically placed on the opposite end of the IC to minimize the source impedance to the gate drive circuits.

5.2.30 Phase C Low-side Source (PC_LS_S)

The phase C low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for phase C.

5.2.31 Phase C Low-side Gate (PC_LS_G)

This is the gate drive for the Phase C low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.32 Phase C High-side Source (PC_HS_S)

The source connection for the Phase C high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.33 Phase C High-side Gate (PC_HS_G)

This is the gate drive for the Phase C high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.34 Phase C Bootstrap (PC_BOOT)

This is the bootstrap capacitor connection for Phase C. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.35 Phase B Low-side Source (PB_LS_S)

The Phase B low-side source is the pin used to return the gate currents from the Low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for Phase B.

5.2.36 Phase B Low-side Gate (PC_LS_G)

This is the gate drive for the Phase B low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.37 Phase B High-side Source (PB_HS_S)

The source connection for the Phase B high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.38 Phase B High-side Gate (PB_HS_G)

This is the gate drive for the Phase B high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.39 Phase B Bootstrap (PB_BOOT)

This is the bootstrap capacitor connection for phase B. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.40 PHASE A Low-side Source (PA_LS_S)

The Phase A low-side source is the pin used to return the gate currents from the low-side FET. Best performance is realized by connecting this node directly to the source of the low-side FET for phase A.

5.2.41 Phase A Low-side Gate (PA_LS_G)

This is the gate drive for the Phase A low-side output FET. It provides high-current through a low-impedance to turn on and off the low-side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

5.2.42 Phase A High-side Source (PA_HS_S)

The source connection for the Phase A high-side output FET is the reference voltage for the gate drive on the high-side FET and also the low-voltage end of the bootstrap capacitor.

5.2.43 Phase A High-side Gate (PA_HS_G)

This is the gate drive for the Phase A high-side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

5.2.44 Phase A Bootstrap (PA_BOOT)

This is the bootstrap capacitor connection for phase A. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the bootstrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V.

5.2.45 VLS Regulator (VLS)

VLS is the gate drive power supply regulated at approximately 15 V. This is an internally generated supply from VPWR. It is the source for the low-side gate drive voltage, and also the High-side bootstrap source. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents, must be connected between this pin and VSS.

5.2.46 VPWR Input (VPWR)

VPWR is the power supply input for VLS and VDD. Current flowing into this input recharges the bootstrap capacitors as well as supplying power to the low-side gate drivers and the VDD regulator. An internal regulator regulates the actual gate voltages. This pin can be connected to system battery voltage if power dissipation is not a concern.

5.2.47 Exposed Pad (EP)

The primary function of the exposed pad is to conduct heat out of the device. This pad may be connected electrically to the substrate of the device.The device performs as specified with the exposed pad un-terminated (floating). However, it is recommended the exposed pad be terminated to pin 29 (VSS) and the system ground.

6 Functional internal block description

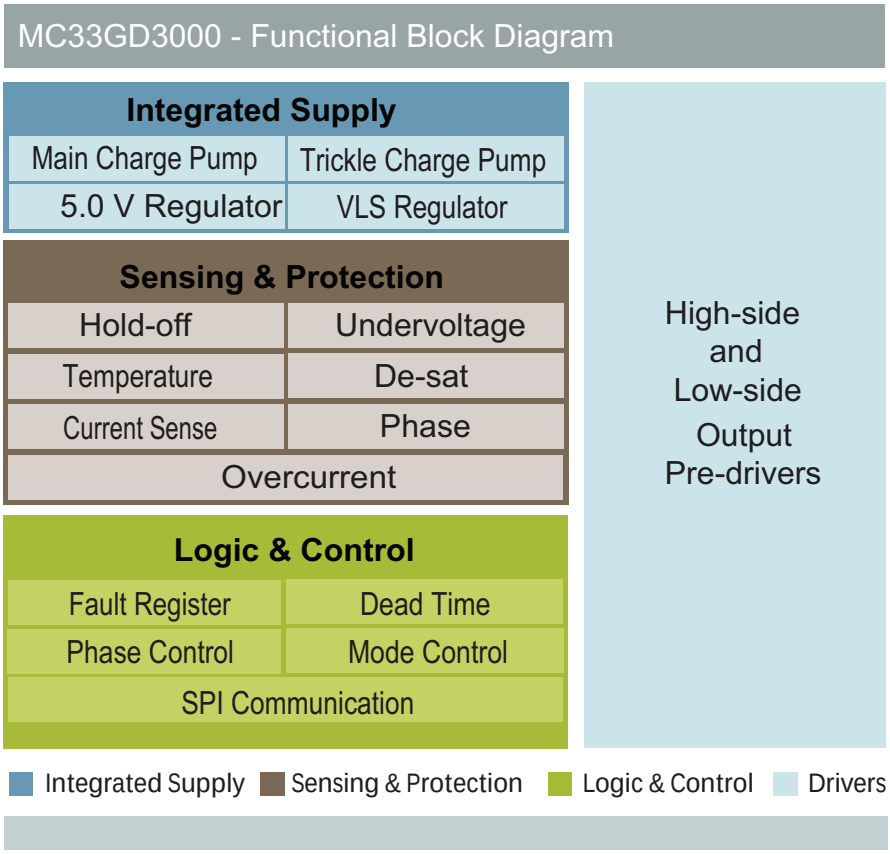


Figure 12. Functional internal block description

All functions of the IC can be described as the following five major functional blocks:

- Logic inputs and interface
- Bootstrap supply
- Low-side drivers
- High-side drivers
- Charge pump

6.1 Logic inputs and interface

This section contains the SPI port, control logic, and shoot-through timers. The IC logic inputs have Schmitt trigger inputs with hysteresis. Logic inputs are 3.0 V compatible. The logic outputs are driven from the internal supply of approximately 5.0 V.

The SPI registers and functionality is described completely in the LOGIC COMMANDS AND REGISTERS section of this document. SPI functionality includes the following:

- **Programming of deadtime delay**—This delay is adjustable in approximately 50 ns steps from 0 ns to 12 µs. Calibration of the delay, because of internal IC variations, is performed via the SPI.
- **Enabling of simultaneous operation of high-side and low-side FETs**—Normally, both FETs would not be enabled simultaneously. However, for certain applications where the load is connected between the high-side and low-side FETs, this could be advantageous. If this mode is enabled, the blanking time delay is disabled. A sequence of commands may be required to enable this function to prevent inadvertent enabling. In addition, this command can only be executed once after reset to enable or disable simultaneous turn-on.
- **Setting of various operating modes** of the IC and enabling of interrupt sources.
  The 33GD3000 allows different operating modes to be set and locked by an SPI command (FULLON, Desaturation Fault, Zero Deadtime). SPI commands can also determine how the various faults are (or are not) reported.

- **Read back of internal registers**.
  The status of the 33GD3000 status registers can be read back by the Master (DSP or MCU).

The $\overline{\text{Px\_HS}}$ and Px_LS logic inputs are edge sensitive. This means the leading edge on an input causes the complementary output to immediately turn off and the selected one to turn on after the deadtime delay as illustrated in Figure 13.

The deadtime delay timer always starts at the time a FET is commanded off and prevents the complementary FET from being commanded on until after the deadtime has elapsed. Commands to turn on the complementary FET after the deadtime has elapsed are executed immediately without any further delay (see Figure 6 and Figure 13).

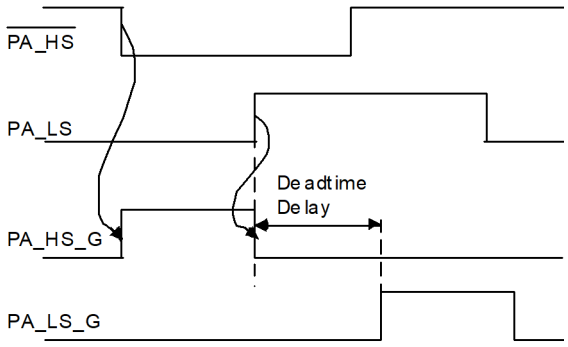


Figure 13. Edge sensitive logic inputs (Phase A)

6.1.1 Low-side and bootstrap supply (VLS)

This is the portion of the IC providing current to recharge the bootstrap capacitors. It also supplies the peak currents required for the low-side gate drivers. The power for the gate drive circuits is provided by VLS which is supplied from the VPWR pin. This pin can be connected to system battery voltage and is capable of withstanding up to the full load dump voltage of the system. However, the IC only requires a low-voltage supply on this pin, typically 13 to 16 V. Higher voltages on this pin increases the IC power dissipation.

In 12 V systems the supply voltage can fall as low as 6.0 V. This limits the gate voltage capable of being applied to the FETs and reduces system performance due to the higher FET on-resistance. To allow a higher gate voltage to be supplied, the IC also incorporates a charge pump. The switches and control circuitry are internal; the capacitors and diodes are external (see Figure 22).

6.1.2 Low-side drivers

These three drivers turn on and off the external low-side FETs. The circuits provide a low-impedance drive to the gate, ensuring the FETs remain off in the presence of high dV/dt transients on their drains. Additionally, these output drivers isolate the other portions of the IC from currents capable of being injected into the substrate due to rapid dV/dt transients on the FET drains.

Low-side drivers switch power from VLS to the gates of the low-side FETs. The low-side drivers are capable of providing a typical peak current of 2.0 A. This gate drive current may be limited by external resistors in order to achieve a good trade-off between the efficiency and EMC (Electro-Magnetic Compatibility) compliance of the application. the low-side driver uses high-side PMOS for turn on and low-side isolated LDMOS for turn off. The circuit ensures the impedance of the driver remains low, even during periods of reduced current. Current limit is blanked immediately after subsequent input state change in order to ensure device stays off during dV/dt transients.

6.1.3 High-side drivers

These three drivers switch the voltage across the bootstrap capacitor to the external high-side FETs. The circuits provide a low-impedance drive to the gate, ensuring the FETs remain off in the presence of high dV/dt transients on their sources. Further, these output drivers isolate the other portions of the IC from currents capable of being injected into the substrate due to rapid dV/dt transients on the FETs.

The high-side drivers deliver power from their bootstrap capacitor to the gate of the external high-side FET, thus turning the high-side FET on. The high-side driver uses a level shifter, which allows the gate of the external high-side FET to be turned off by switching to the high-side FET source.

The gate supply voltage for the high-side drivers is obtained from the bootstrap supply, so, a short time is required after the application of power to the IC to charge the bootstrap capacitors. To ensure this occurrence, the internal control logic does not allow a high-side switch to be turned on after entering the ENABLE state until the corresponding low-side switch is enabled at least once. Caution must be exercised after a long period of inactivity of the low-side switches to verify the bootstrap capacitor is not discharged. It is charged by activating the low-side switches for a brief period, or by attaching external bleed resistors from the HS_S pins to GND. See Initialization requirements on page 39.

In order to achieve a 100% duty cycle operation of the high-side external FETs, a fully integrated trickle charge pump provides the charge necessary to maintain the external FET gates at fully enhanced levels. The trickle charge pump has limited ability to supply external leakage paths while performing it's primary function. The graph in Figure 11 shows the typical margin for supplying external current loads. These limits are based on maintaining the voltage at CBOOT at least 3.0 V greater than the voltage on the HS_S for this phase. If this voltage differential becomes less than 3.0 V, the corresponding high-side FET most likely does not remain fully enhanced and the high-side driver may malfunction due to insufficient bias voltage between CBOOT and HS_S.

The slew rate of the external output FET is limited by the driver output impedance, overall (external and internal) gate resistance and the load capacitance. To ensure the low-side FET is not turned on by a large positive dV/dt on the drain of the low-side FET, the turn-on slew rate of the high-side should be limited. If the slew rate of the high-side is limited by the gate-drain capacitance of the high-side FET, then the displacement current injected into the low-side gate drive output is approximately the same value. Therefore, to ensure the low-side drivers can be held off, the voltage drop across the low-side gate driver must be lower than the threshold voltage of the low-side FET (see Figure 14).

Similarly, during large negative dV/dt, the high-side FET is able to remain off if its gate drive Low-side switch, develops a voltage drop less than the threshold voltage of the high-side FET. The gate drive low-side switch discharges the gate to the source.

Additionally, during negative dV/dt the low-side gate drive could be forced below ground. The low-side FETs must not inject detrimental substrate currents in this condition.

The occurrence of these cases depends on the polarity of the load current during switching.

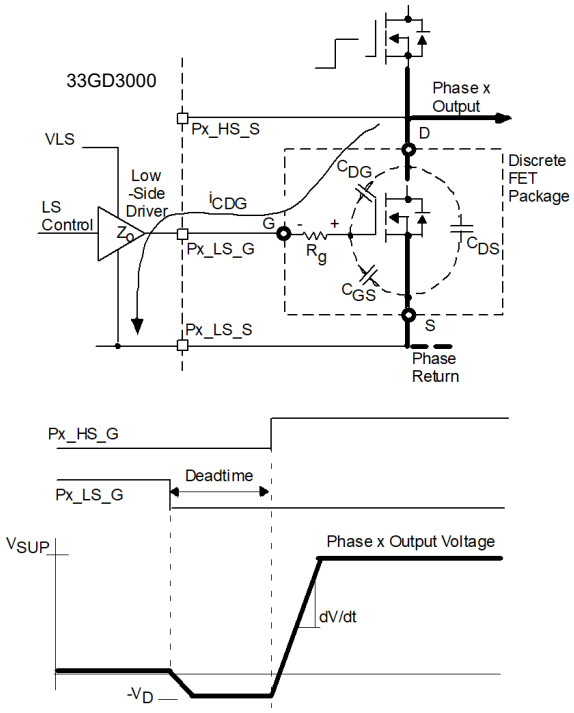


Figure 14. Positive dV/dt transient

6.1.4 Driver fault protection

The 33GD3000 integrates several protection mechanisms against various faults. The first of them is the Current Sense Amplifier with the Overcurrent Comparator. These two blocks are common for all three driver phases.

6.1.4.1 Current sense amplifier

This amplifier is usually connected as a differential amplifier (see Figure 9). It senses a current flowing through the external FETs as a voltage across the current sense resistor R_{SENSE}. Since the amplifier common mode range does not extend below ground, it is necessary to use an external reference to permit measuring both positive and negative currents.

The amplifier output can be monitored directly (e.g. by the microcontroller's ADC) at the AMP_OUT pin, providing the means for closed loop control with the 33GD3000. The output voltage is internally compared with the Overcurrent Comparator threshold voltage (see Figure 22).

6.1.4.2 Overcurrent comparator

The amplified voltage across R_{SENSE} is compared with the pre-set threshold value by the overcurrent comparator input. If the Current Sense Amplifier output voltage exceeds the threshold of the Overcurrent Comparator it would change the status of its output (OC_OUT pin) and the fault condition would be latched (see Figure 18).

The occurrence of this fault would be signaled by the return value of the Status Register 0. If the proper Interrupt Mask has been set, this fault condition generates an interrupt - the INT pin asserts High. The INT is held in the High state until the fault is removed, and the appropriate bit in the Status Register 0 is cleared by the CLINT0 command. This fault reporting technique is described in detail in the Logic commands and registers section.

6.1.4.3 Desaturation detector

The Desaturation Detector is a comparator integrated into the output driver of each phase channel. It provides an additional means to protect against “Short-to-Ground” fault condition. A short to ground is detected by an abnormally high-voltage drop in VDS of the high-side FET. Note that if the gate-source voltage of the high-side FET drops below saturation, the device goes into linear mode of conduction which can also cause a desaturation error.

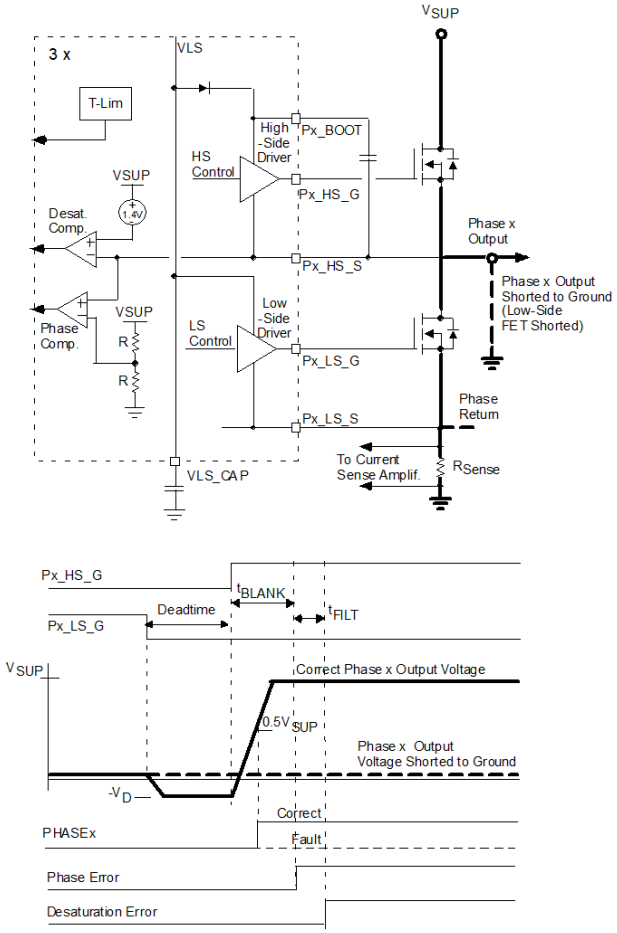


Figure 15. Short to ground detection

When switching from low-side to high-side, the high-side is commanded On after the end of the deadtime. The deadtime period starts when the low-side is commanded Off. If the voltage at Px_HS_S is less than 1.4 V below V_{SUP} after the blanking time (t_{BLANK}) a desaturation fault is initiated. An additional 1.0 µs digital filter is applied from the initiation of the desaturation fault before it is registered, and all phase drivers are turned Off (Px_HS_G clamped to Px_HS_S and Px_LS_G clamped to Px_LS_S). If the desaturation fault condition clears before the filter time expires, the fault is ignored and the filter timer resets.

Valid faults are registered in the fault status register, which can be retrieved by way of the SPI. Additional SPI commands mask the INT flag and disable output stage shutdown, due to desaturation and phase errors. See Logic commands and registers section for details on masking INT behavior and disabling the protective function.

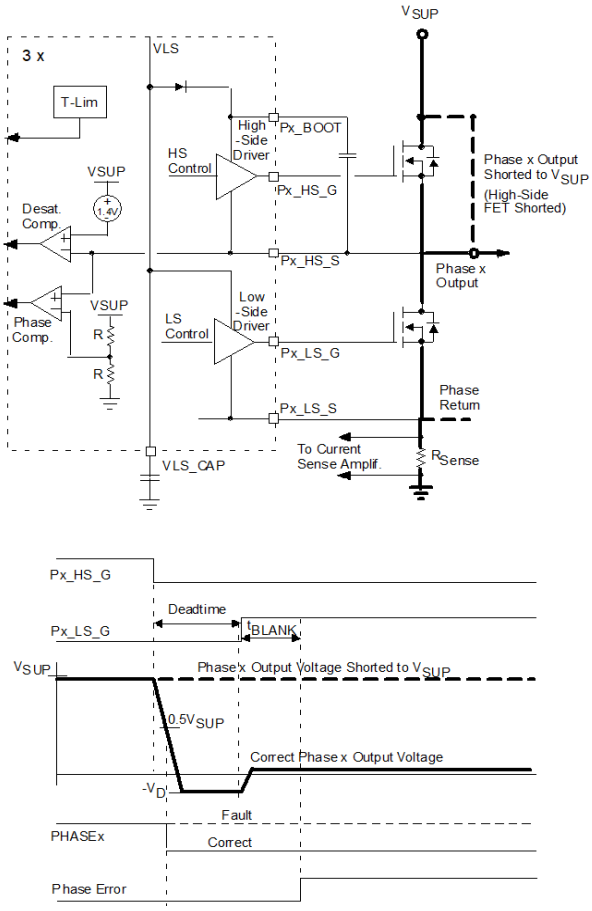


Figure 16. Short to supply detection

6.1.4.4 Phase comparator

Faults could also be detected as Phase Errors. A phase error is generated if the output signal (at Px_HS_S) does not properly reflect the drive conditions.

A phase error is detected by a Phase Comparator. The Phase Comparator compares the voltage at the Px_HS_S node with a reference of one half the voltage at the VSUP pin. A high-side phase error (which also triggers the Desaturation Detector) occurs when the high-side FET is commanded on, and Px_HS_S is still *low* at the end of the deadtime and blanking time duration. Similarly, a LS phase error occurs when the low-side FET is commanded on, and the Px_HS_S is still high at the end of the deadtime and blanking time duration.

The Phase Error Flag is the triple OR of phase errors from each phase. Each phase error is the OR of the high-side and low-side phase errors. This flag can generate an interrupt if the appropriate mask bit is set. The INT is held in the High state until the fault is removed, and the appropriate bit in the Status Register 0 is cleared by the CLINT1 command. This fault reporting mechanism is described in detail in the Logic commands and registers section.

6.1.5 VLS undervoltage

Since VLS supplies both the gate driver circuits and the gate voltage, it is critical it maintains sufficient potential to place the power stage FETs in saturation. Since proper operation cannot continue with insufficient levels, a low VLS condition shuts down driver operation. The VLS Under Voltage threshold is between 7.5 V and 8.5 V. When a decreasing level reaches the threshold, both the HS and the LS output gate circuit drive the gates OFF for about 8 us before reducing the drive to hold off levels. Since low VLS is a condition for turning on the Hold Off circuit, Hold Off then provides a weak pull-down on all gates. A filter timeout of about 700 ns ensures noise on VLS does not cause premature protective action.

When VLS rises above this threshold again, the LS Gate immediately follows the level of the input. However, a short initialization sequence must be executed to restore operation of the HS Gate (see Initialization requirements on page 39). Since VLS is no longer undervoltage, the Hold Off circuit is turned off and the HS Gate is in a high-impedance state until the LS Gate responds to an input command to turn off.

6.1.6 Hold off circuit

The IC guarantees the output FETs are turned off in the absence of V_{DD} or V_{PWR} by means of the hold off circuit. A small current source, generated from VSUP, typically 100 µA, is mirrored and pulls all the output gate drive pins low when V_{DD} is less than about 3.0 V, $\overline{RST}$ is active (low), or when VLS is lower than the VLS_Disable threshold. A minimum of 3.0 V is required on VSUP to energize the hold off circuit.

6.1.7 Charge pump

The Charge Pump circuit provides the basic switching elements required to implement a charge pump, when combined with external capacitors and diodes for enhanced low-voltage operation.

When the 33GD3000 is connected per the typical application using the charge pump (see Figure 22), the regulation path for VLS includes the charge pump and a linear regulator. The regulation set point for the linear regulator is nominally at 15.34 V. As long as VLS output voltage (VLS_{OUT}) is greater than the VLS analog regulator threshold (VLS_{ATH}) minus V_{THREG}, the charge pump is not active.

If $VLS_{OUT} < VLS_{ATH} – V_{THREG}$ the charge pump turns ON until $VLS_{OUT} > VLS_{ATH} – V_{THREG} + V_{HYST.}$ V_{HYST} is approximately 200 mV. VLS_{ATH} does not interfere with this cycle even when there is overlap in the thresholds, due to the design of the regulator system.

The maximum current the charge pump can supply is dependent on the pump capacitor value and quality, the pump frequency (nominally 130 kHz), and the Rdson of the pump FETs. The effective charge voltage for the pump capacitor would be $V_{SYS} – 2 * V_{DIODE}$. The total charge transfer would then be $C_{PUMP} * (V_{SYS} – 2*V_{DIODE})$. Multiplying by the switch frequency gives the theoretical current the pump can transfer: $F_{PUMP} * C_{PUMP} * (V_{SYS} – 2*V_{DIODE})$.

NOTE: There is also another smaller, fully integrated charge pump (Trickle Charge Pump - see Figure 2), which is used to maintain the high-side drivers' gate V_{GS} in 100 percent duty cycle modes.

7 Functional device operation

7.1 Operational modes

7.1.1 Reset and enable

The 33GD3000 has three power modes of operation described in Table 6. There are three global control inputs ($\overline{RST}$, EN1, EN2), which together with the status of VDD, VLS and DESAT/PHASE faults control the behavior of the IC.

The operating status of the IC can be described by the following five modes:

- **Sleep mode** - When $\overline{RST}$ is low, the IC is in Sleep mode. The current consumption of the IC is at minimum.
- **Standby mode** - The $\overline{RST}$ input is high while one of the Enable inputs is low. The IC is fully biased up and operating, all the external FETs are actively turned off by both high-side and low-side gate drives. The IC is ready to enter the Enable mode.
- **Initialization mode** - When EN1, EN2 and $\overline{RST}$ all go high, the device enters the Initialization mode. Toggling the LS and then the HS initializes the driver and normal operation in the Enable mode begins (see Initialization requirements on page 39).
- **Enable mode** - After initialization is complete, the device goes into the Enable mode and operates normally. Normal operation continues in this mode as long as both enable pins and $\overline{RST}$ are high.
- **Fault Protection mode** - If a protective fault occurs (either Desat/Phase or VLS UV) the device enters a Fault Protection mode. After a fault clears, the device requires initialization again before resuming normal Enable mode operation.

Table 6. Functions of $\overline{RST}$, EN1 and EN2 pins

$\overline{RST}$	EN1, EN2	Mode of operation (driver condition)
0	xx	**Sleep mode** - in this mode (low quiescent current) the driver output stage is switched-off with a weak pull-down. All error and SPI registers are cleared. The internal 5.0 V regulator is turned off and VDD is pulled low. All logic outputs except SO are clamped to VSS.
1	0x x0	**Standby mode** - IC fully biased up and all functions are operating, the output drivers actively turn off all of the external FETs (after initialization). The SPI port is functional. Logic level outputs are driven with low-impedance. SO is high-impedance unless $\overline{CS}$ is low. V_{DD}, Charge Pump and V_{LS} regulators are all operating. The IC is ready to move to Enable mode.
1	11	**Initialization mode** - Low-side drivers are enabled, SPI is fully operational. Ready for initialization (see Initialization requirements on page 39). **Enable mode** - (normal operation). Drivers are enabled; output stages follow the input command. After Enable, outputs require a pulse on Px_LS before corresponding HS outputs turns on in order to charge the bootstrap capacitor. All error pin and register bits are active if detected. **Fault Protection mode** - Drivers are turned OFF or disabled per the fault and protection mode registers. Recovery requires initialization (see Initialization requirements on page 39).

Table 7. Functional ratings

(T_J = -40 °C to 150 °C and supply voltage range V_{SUP} = V_{PWR} = 5.0 to 45 V, C = 0.47 µF)

Characteristic	Value
Default State of input pin Px_LS, EN1, EN2, $\overline{RST}$, SI, SCLK, if left open [58] (Driver output is switched off, high-impedance mode)	Low (<1.0 V)
Default State of input pin $\overline{Px\_HS}$, $\overline{CS}$ if left open [58] (Driver output is switched off, high-impedance mode)	High (>2.0 V)

Notes

58. To assure a defined status for all inputs, these pins are internally biased by pull-up/down current sources.

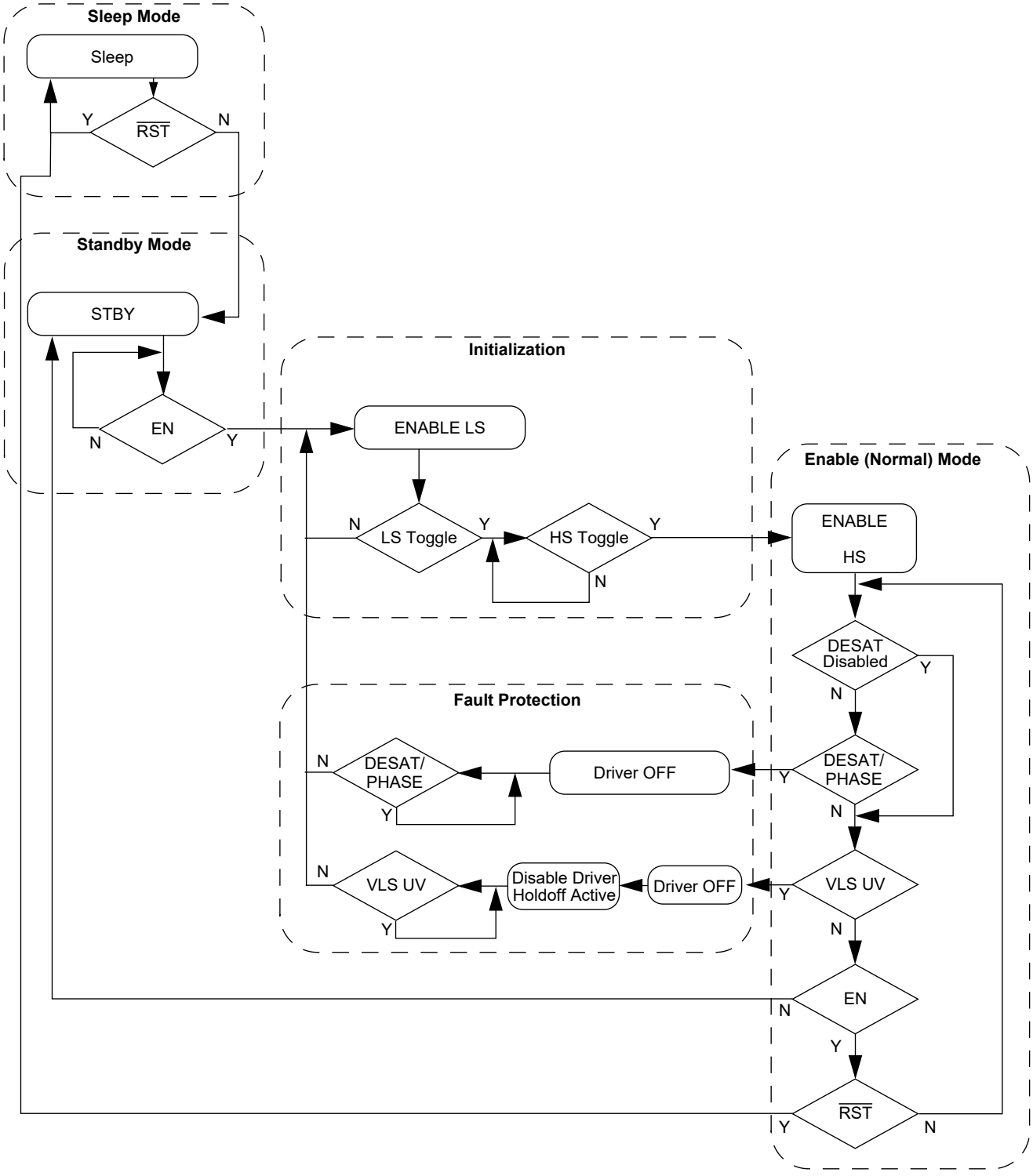


Figure 17. Device operational flow diagram

7.2 Logic commands and registers

7.2.1 Command descriptions

The IC contains internal registers to control the various operating parameters, modes, and interrupt characteristics. These commands are sent and status is read via 8-bit SPI commands. The IC uses the last eight bits in an SPI transfer, so devices can be daisy-chained. The first three bits in an SPI word can be considered to be the Command with the trailing five bits being the data.

The SPI logic generates a framing error and ignore the SPI message if the number of received bits is not eight or if it is not a multiple of eight. After $\overline{RST}$, the first SPI result returned is Status Register 0.

Table 8. Command List

Command	Name	Description
000x xxxx	NULL	These commands are used to read IC status. These commands do not change any internal IC status. Returns Status Register 0-3, depending on sub command.
0010 xxxx	MASK0	Sets a portion of the interrupt mask using lower four bits of command. A “1” bit enables interrupt generation for this flag. INT remains asserted if uncleared faults are still present. Returns Status Register 0.
0011 xxxx	MASK1	Sets a portion of the interrupt mask using lower four bits of command. A “1” bit enables interrupt generation for this flag. INT remains asserted if uncleared faults are still present. Returns Status Register 0.
010x xxxx	Mode	Enables Desat/Phase Error mode. Enables FULLON mode. Locks further mode changes. Returns Status Register 0.
0110 xxxx	CLINT0	Clears a portion of the fault latch corresponding to MASK0 using lower four bits of command. A 1 bit clears the interrupt latch for this flag. INT remains asserted if other unmasked faults are still present. Returns Status Register 0.
0111 xxxx	CLINT1	Clears a portion of the fault latch corresponding to MASK1 using lower four bits of command. A 1 bit clears the interrupt latch for this flag. INT remains asserted if other unmasked faults are still present. Returns Status Register 0.
100x xxxx	DEADTIME	Set deadtime with calibration technique. Returns Status Register 0.

7.2.2 Fault reporting and interrupt generation

Different fault conditions described in the previous chapters can generate an interrupt - INT pin output signal asserted high. When an interrupt occurs, the source can be read from Status Register 0, which is also the return word of most SPI messages. Faults are latched on occurrence, and the interrupt and faults are only cleared by sending the corresponding CLINTx command. A fault which still exists continues to assert an interrupt.

Note: If there are multiple pending interrupts, the INT line does not toggle when one of the faults is cleared. Interrupt processing circuitry on the host must be level sensitive to correctly detect multiple simultaneous interrupt.

Thus, when an interrupt occurs, the host can query the IC by sending a NULL command; the return word contains flags indicating any faults not cleared since the CLINTx command was last written (rising edge of $\overline{CS}$) and the beginning of the current SPI command (falling edge of $\overline{CS}$). The NULL command causes no changes to the state of any of the fault or mask bits. The logic clearing the fault latches occurs only when:

1. A valid command had been received(i.e. no framing error);
2. A state change did not occur during the SPI message (if the bit is being returned as a 0 and a fault change occurs during the middle of the SPI message, the latch remains set). The latch is cleared on the trailing (rising) edge of the $\overline{CS}$ pulse.
   Note, to prevent missing any faults the CLINTx command should not generally clear any faults without being observed; i.e. it should only clear faults returned in the prior NULL response.

7.2.3 NULL commands

This command is sent by sending binary 000x xxxx data. This can be used to read IC status in the SPI return word. Message 000x xx00 reads Status Register 0. Message 000x xx01 through 000x xx11 read additional internal registers.

Table 9. NULL Commands

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	0	0	x	x	x	0	0
Reset								

NULL Commands are described in detail in the STATUS REGISTERS section of this document.

7.2.3.1 MASK command

This is the mask for interrupts. A bit set to “1” enables the corresponding interrupt. Because of the number of MASK bits, this register is in two portions:

1. MASK0
2. MASK1

Both are accessed with 0010 xxxx and 0011 xxxx patterns respectively. Figure 18 illustrates how interrupts are enabled and faults cleared. CLINT0 and CLINT1 have the same format as MASK0 and MASK1 respectively, but the action is to clear the interrupt latch and status register 0 bit corresponding to the lower nibble of the command.

Table 10. MASK0 register

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	0	1	0	x	x	x	x
Reset					1	1	1	1

7.2.3.2 Interrupt handling

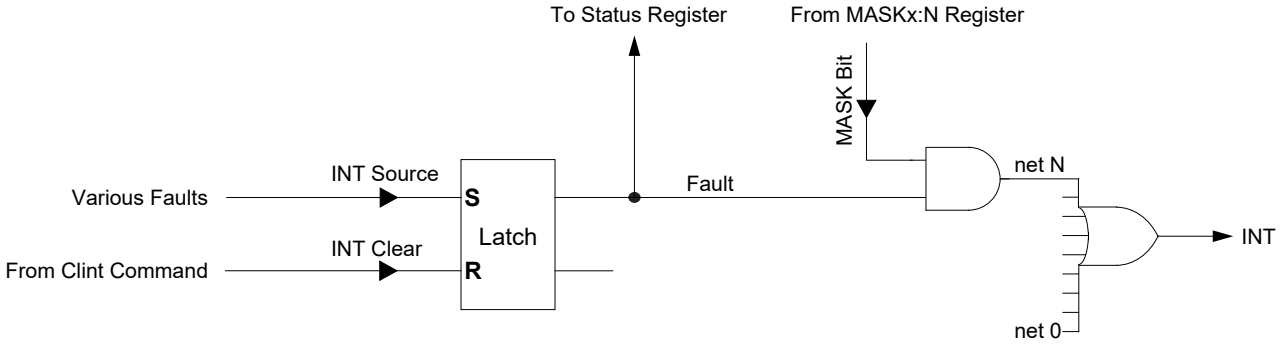


Figure 18. Interrupt handling

Table 11. MASK1 register

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	0	1	1	x	x	x	x
Reset					1	1	1	1

Table 12. Setting interrupt masks

Mask:bit	Description
MASK0:0	**Overtemperature** on any gate drive output generates an interrupt if this bit is set.
MASK0:1	**Desaturation** event on any output generates an interrupt if this bit is set.
MASK0:2	**VLS undervoltage** generates an interrupt if this bit is set.
MASK0:3	**Overcurrent Error**–if the overcurrent comparator threshold is exceeded, an interrupt is generated.
MASK1:0	**Phase Error**–if any Phase comparator output is not at the expected value when an output is command on, an interrupt is generated. This signal is the XOR of the phase comparator output with the output drive state, and blacked for the duration of the desaturation blanking interval. In FULLON mode, this signal is blanked and cannot generate an error.
MASK1:1	**Framing Error**–if a framing error occurs, an interrupt is generated.
MASK1:2	**Write Error** after locking.
MASK1:3	**Reset Event**–If the IC is reset or disabled, an interrupt occurs. Since the IC always starts from a reset condition, this can be used to test the interrupt mechanism because when the IC comes out of RESET, an interrupt immediately occurs.

7.2.4 MODE command

This command is sent by sending binary 010x xxxx data.

Table 13. MODE command

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	1	0	0	Desaturation Fault Mode	0	FULLON Mode	Mode Lock
Reset					0	0	0	0

- **Bit 0**–**Mode Lock** is used to enable or disable Mode Lock. This bit can only be cleared with a device reset. Since the mode Lock mode can only be set, this bit prevents any subsequent, and likely erroneous, mode, deadtime, or mask register changes from being received. If an attempt is made to write to a register when Mode Lock is enabled, a Write Error fault is generated.
- **Bit 1**–**FULLON mode.** If this bit is set, programmed deadtime control is disabled, making it is possible to have both high and Low-side drivers in a phase on simultaneously. This could be useful in special applications such as alternator regulators, or switched-reluctance motor drive applications. There is no deadtime control in FULLON mode. Input signals directly control the output stages, synchronized with the internal clock.
  This bit is a “0”, after RESET. Until overwritten, the IC operates normally; deadtime control and logic prevents both outputs from being turned on simultaneously.
- **Bit 3**– **Desaturation Fault mode** controls what happen when a desaturation event is detected. When set to “0”, any desaturation on any channel causes all six output drivers to shutoff. The drivers can only be re-enabled by executing the CLINT command. When 1, desaturation faults are completely ignored.
  Bit 3 controls behavior if a Desaturation, or Phase Error event is detected. The possibilities are:
  — 0: Default: When a Desaturation, or Phase Error event is detected on any channel, all channels turn off and generates an Interrupt, if interrupts are enabled.
  — 1: Disable: Desaturation /Phase Error channel shutdown is disabled, but interrupts are still possible if unmasked.

Sending a MODE command and setting the Mode Lock simultaneously are allowed. This sets the requested mode and locks out any further changes.

7.2.5 DEADTIME command

Deadtime prevents the turn-on of both transistors in the same phase until the deadtime has expired. The deadtime timer starts when a FET is commanded off (see Figure 6 and Figure 13). The deadtime control is disabled by enabling the FULLON mode.

The deadtime is set by sending the DEADTIME command (100x xxx1), and then sending a calibration pulse of $\overline{CS}$. This pulse must be 16 times longer than the required deadtime (see Figure 19). Deadtime is measured in cycle times of the internal time base, f_{TB}. This measurement is divided by 16 and stored in an internal register to provide the reference for timing the deadtime between high and low gate transactions in the same phase.

For example: the internal time base is running at 20 MHz and a 1.5 µs deadtime is required. First a DEADTIME command is sent (using the SPI), then a $\overline{CS}$ is sent. The $\overline{CS}$ pulse is 16*1.5 = 24 µs wide. The IC measures this pulse as 24000 ns/50 ns = 480 clock cycles and stores 480/16 = 30 in the deadtime register. Until the next deadtime calibration is performed, 30 clock cycles separate the turn off and turn on gate signals in the same phase. The worst case error immediately after calibration is +0/-1 time base cycle, for this example +0 ns/-50 ns. Note that if the internal time base drifts, the effect on dead time scales directly.

Sending a ZERO DEADTIME command (100x xxx0) sets the deadtime timer to 0. However, simultaneous turn-on of high-side and low-side FETs in the same phase is still prevented unless the FULLON command has been transmitted. There is no calibration pulse expected after receiving the ZERO DEADTIME command.

After RESET, deadtime is set to the maximum value of 255 time base cycles (typically 15 µs).

The IC ignores any SPI data which is sent during the calibration pulse. If there are any transitions on SI or SCLK while the Deadtime $\overline{CS}$ pulse is low, a Framing Error is generated, however, the $\overline{CS}$ pulse is used to calibrate the deadtime

Table 14. .DEADTIME command

SPI Data Bits	7	6	5	4	3	2	1	0
Write	1	0	0	x	x	x	x	ZERO/ CALIBRATE
Reset					x	x	x	x

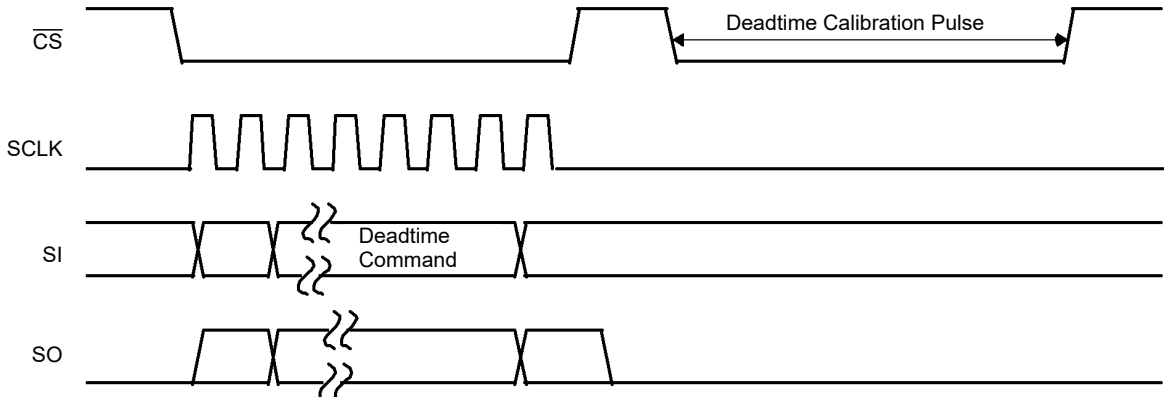


Figure 19. Deadtime calibration

7.2.6 Status registers

After any SPI command, the status of the IC is reported in the return value from the SPI port. There are four variants of the NULL command used to read various status in the IC. Other commands return a general status word in the Status Register 0.

There are four Status Registers in the IC. Status Register 0 is most commonly used for general status. Registers one through three are used to read or confirm internal IC settings.

7.2.6.1 Status Register 0 (Status Latch Bits)

This register is read by sending the NULL0 command (000x xx00). It is also returned after any other command. This command returns the following data:

Table 15. Status Register 0

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 0 Read	RESET Event	Write Error	Framing Error	Phase Error	Overcurrent	Low VLS	DESAT Detected on any Channel	TLIM Detected on any Channel
Reset	1	0	0	0	0	0	0	0

All status bits are latched. The latches are cleared only by sending a CLINT0 or CLINT1 command with the appropriate bits set. If the status is still present, this bit does not clear. CLINT0 and CLINT1 have the same format as MASK0 and MASK1 respectively.

- **Bit 0**–is a flag for **Overtemperature** on any channel. This bit is the OR of the latched three internal TLIM detectors.This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 1**–is a flag for **Desaturation Detection** on any channel. This bit is the OR of the latched three internal high-side desaturation detectors and phase error logic. Faults are also detected on the low-side as phase errors. A phase error is generated if the output signal (at Px_HS_S) does not properly reflect the drive conditions. The phase error is the triple OR of phase errors from each phase. Each phase error is the OR of the HS and LS phase errors. An HS phase error (which also triggers the desaturation detector) occurs when the HS FET is commanded on, and the Px_HS_S is still *low* in the deadtime duration after it is driven ON. Similarly, a LS phase error occurs when the LS FET is commanded on, and the Px_HS_S is still high in the deadtime duration after the FET is driven ON. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 2**– is a flag for **Low Supply Voltage**. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 3**–is a flag for the output of the **Overcurrent Comparator**. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 4**–is a flag for a **Phase Error**. If any Phase comparator output is not at the expected value when just one of the individual high or low-side outputs is enabled, the fault flag is set. This signal is the XOR of the phase comparator output with the output driver state, and blanked for the duration of the desaturation blanking interval. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 5**–is a flag for a **Framing Error**. A framing error is a SPI message not containing one or more multiples of eight bits. SCLK toggling while measuring the Deadtime calibration pulse is also a framing error. This would typically be a transient or permanent hardware error, perhaps due to noise on the SPI lines. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 6**–indicates a **Write Error After the Lock** bit is set. A write error is any attempted write to the MASKn, Mode, or a Deadtime command after the Mode Lock bit is set. A write error is any attempt to write any other command than the one defined in the Table 8. This would typically be a software error. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 7**–is set upon **exiting $\overline{\text{RST}}$**. It can be used to test the interrupt mechanism or to flag for a condition where the IC gets reset without the host being otherwise aware. This flag can generate an interrupt if the appropriate mask bit is set.

7.2.6.2 Status Register 1 (MODE Bits)

This register is read by sending the NULL1 command (000x xx01). This is guaranteed to not affect IC operation and returns the following data:

Table 16. Status Register 1

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 1 Read	0	Desaturation Mode	Zero Deadtime Set	Calibration Overflow	Deadtime Calibration	0	FULLON Mode	Lock Bit
Reset	0	0	0	0	0	0	0	0

- **Bit 0**–**Lock Bit** indicates the IC registers (Deadtime, MASKn, CLINTn, and Mode) are locked. Any subsequent write to these registers is ignored and sets the Write Error flag.
- **Bit 1**– is the present status of **FULLON mode**. If this bit is set to “0”, the FULLON mode is not allowed. A “1” indicates the IC can operate in FULLON mode (both high-side and low-side FETs of one phase can be simultaneously turned on).
- **Bit 3**–indicates **Deadtime Calibration** occurred. It is “0” until a successful Deadtime command is executed. This includes the Zero Deadtime setting, as well as a Calibration Overflow.
- **Bit 4**–is a flag for a Deadtime **Calibration Overflow**.
- **Bit 5**–is set if **Zero Deadtime** is commanded.
- **Bit 6**–reflects the current state of the **Desaturation/Phase Error turn-off** mode.

7.2.6.3 Status Register 2 (MASK bits)

This register is read by sending the NULL2 command (000x xx10). This is guaranteed to not affect IC operation and returns the following data:

Table 17. Status Register 2

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 2 Read	Mask1:3	Mask1:2	Mask1:1	Mask1:0	Mask0:3	Mask0:2	Mask0:1	Mask0:0
Reset	1	1	1	1	1	1	1	1

7.2.6.4 Status Register 3 (Deadtime)

This register is read by sending the NULL3 command (000x xx11). This is guaranteed to not affect IC operation and returns the following data:

Table 18. Status Register 3

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 3 Read	Dead7	Dead6	Dead5	Dead4	Dead3	Dead2	Dead1	Dead0
Reset	0	0	0	0	0	0	0	0

These bits represent the calibration applied to the internal oscillator to generate the requested deadtime. If calibration is not yet performed, all these bits return 0 even though the actual dead time is the maximum.

7.3 Initialization requirements

The 33GD3000 provides safe, dependable gate control for 3 phase BLDC motor control units when it is properly configured. However, if improperly initialized, the high-side gate drive can be left in a high-impedance mode which allows charge to accumulate from external sources, eventually turning on the high-side output transistor. It is prudent to follow a well defined initialization procedure which establishes known states on the gates of all the phase drivers before any current flows in the motor.

7.3.1 Recovery from Sleep mode (RESET)

The output gate drive is pulled low with the hold off circuit as long as VLS is low, there is a Power On Reset condition or +5.0 V is low. These conditions are present during a Reset condition. When first coming out of a reset condition, the gate drive circuits are in a high-impedance state until the first command is given for operation. After the Reset line goes high, the supplies begin to operate and the hold off circuit is deactivated. The phase input lines do not have any effect on the gate drive until both ENABLE1 and ENABLE2 go high and even then, the low-side gate must be commanded on before the high-side gate can be operated. This is to ensure the bootstrap capacitor has been charged before commencing normal operation. Then the high-side gate must be commanded on and then off to initialize the output latches. A proper initialization sequence places the output gate drives in a low-impedance known condition prior to releasing the device for normal operation.

A valid initialization sequence would go something like this:

1. RESET goes high (ENABLE1 and ENABLE2 remain low)
2. SPI commands to configure valid interrupts, DESAT mode and Dead Time are issued
3. SPI command to clear all interrupt conditions
4. ENABLE1 and ENABLE2 are set HIGH (LS outputs are now enabled)
5. PA_LS, PB_LS and PC_LS are toggled HIGH for about 1us (HS outputs are enabled, but not latched)
6. Toggle nPA_HS, nPB_HS and nPC_HS LOW for DEAD TIME plus at least 0.1 μs (HS outputs are now latched and operational).

End of initialization.

Doing step 6 simultaneously on all HS inputs places the motor into High-side Recirculation mode and does not cause motion during the time they are ON. This action forces the high-side gate drive out of tri-state mode and leave it with the HS_G shorted to HS_S on all phases. The HS output FETs is OFF and ready for normal motor control.

Step 5 and step 6 can be done on all the stated inputs simultaneously. It may be desirable for the HS (step 6) to be toggled simultaneously to prevent current from flowing in the motor during initialization.

Note the inputs PA_LS, PB_LS, PC_LS, nPA_HS, nPB_HS and nPC_HS are edge sensitive. Toggling the LS inputs enables the HS drivers, so for the HS drivers to be initialized correctly the edge of the input signal to the HS drivers must come after the LS input toggle. A failure to do this results in the HS gate output remaining in a High-impedance mode. This can result in an accumulation of charge, from internal and external leakage sources, on the gate of the HS output FET causing it to turn ON even though the input level to the 33GD3000 would appear to indicate it should be OFF.

When this happens, the logic of the 33GD3000 allows the LS output FET to be turned ON without taking any action on the HS gate because the logic is still indicating the HS gate is OFF. The initial LS input transition from low to high needs to be after both ENABLE inputs are high (the device in Normal mode) for the same reason. The delay between ENABLE and the LS input should be 280 ns minimum to ensure the device is out of STBY mode. Once initialized the output gate drives continues to operate in a Low-impedance mode as commanded by the inputs until the next reset event.

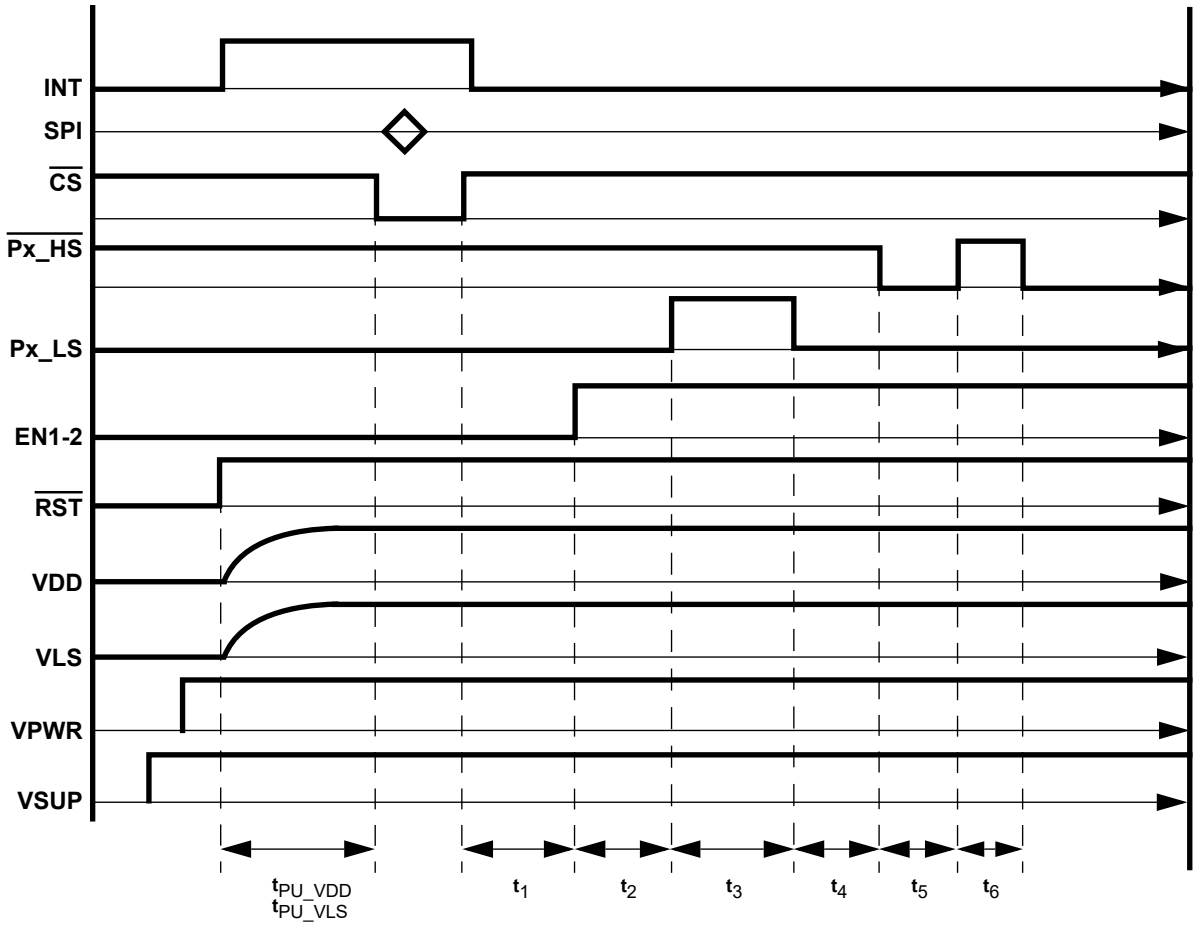


Figure 20. Full initialization

Table 19. Full initialization timing description

Time	Description	Min.	Comments
t_{PU_VDD}, t_{PU_VLS}	Power up time from RESET	2.0 ms	RESET must remain high long enough for VDD and VLS to reach the full regulated voltage. The normal time for this to occur is specified as 2.0 ms maximum. If there is more capacitance on VLS or VDD than the normal values given in the specification, this time may need to be increased. In general, the time may be safely scaled linearly with the capacitance. If the charge pump is used it may also increase this time. An estimate of increased time, due to the charge pump, would be to add 25%. For example, the nominal VLS capacitance is 2.2 µF on each pin, the power up time should be increased to 4.0 ms, 5.0 ms if using the charge pump.
t_1	End of SPI communication to EN1 and EN2 rising edge	0 ns	
t_2	EN1 and EN2 rising edge to first LS output command	280 ns	Restricted by EN1 and EN2 propagation delay
t_3	Initial LS ON period	1.0 µs	Nominally 1.0 µs is more than enough. The calculated value is $5*C_{BOOT}(R_{SENSE} + R_{DSON\_LS})$. 100 ns for default recovery.

Table 19. Full initialization timing description

Time	Description	Min.	Comments
t_4	LS OF to HS ON	0 ns	No defined maximum, but HS is undefined until beginning of toggle on the HS
t_5	Initial HS ON period	100 ns + dead time	Minimum: Dead-time + 100 ns to guarantee the HS is switched. Maximum: Same limitations as normal operation. Unlimited time if leakage currents are less than trickle charge pump margin.
t_6	HS OFF to Normal Operation	0 ns	Immediately begin normal operation

7.3.2 Recovery from Standby mode or a fault

When the 33GD3000 is placed in Standby mode or a fault condition causes a shutdown, the gate outputs are all driven low. The high-side gate drive is then disabled and locked to prevent unauthorized transitions. This requires an initialization sequence to recover normal operation at the end of this mode of operation. The initialization sequence is nearly identical to recovery from Sleep mode, with the modification that the initial pulse to the low-side control inputs can be reduced to a 100 ns pulse (the low-side gates may not actually change state). Then the initialization is completed by cycling the high-side gates to re-engage the gate drive and ensure it is in the proper state prior to resuming normal operation.

A valid initialization sequence would go something like this:

1. SPI command to clear all interrupt conditions
2. ENABLE1 and ENABLE2 are set HIGH (LS outputs are now enabled)
3. PA_LS, PB_LS and PC_LS are toggled HIGH for at least 100 ns (HS Gate Drive outputs are enabled) longer if bootstrap capacitors need charged.
4. Toggle nPA_HS, nPB_HS and nPC_HS LOW for DEAD TIME plus at least 100 ns.

End of initialization.

Doing step 4 simultaneously on all HS inputs, places the motor into High-side Recirculation mode and does not cause motion during the time they are ON.

This action restores the high-side gate drive operation and leave it with the HS_G shorted to HS_S on all phases. The HS output FETs is OFF and ready for normal motor control.

Step 3 and step 4 can be done on all the stated inputs simultaneously. In fact it is desirable for the HS (step 4) to be toggled simultaneously to prevent current from flowing in the motor during initialization.

Note the inputs PA_LS, PB_LS, PC_LS, nPA_HS, nPB_HS and nPC_HS are edge sensitive. Toggling the LS inputs enables the HS drivers, so for the HS drivers to be initialized correctly the edge of the input signal to the HS drivers must come after the LS input toggle. A failure to do this results in the HS gate output remaining locked out from input control. The initial LS input transition from low to high needs to be after both ENABLE inputs are high (the device in Normal mode) for the same reason. The delay between ENABLE and the LS input should be 280 ns minimum to ensure the device is out of STBY mode.

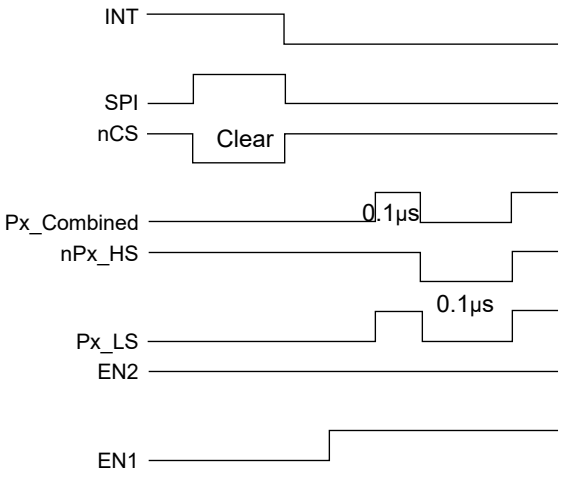


Figure 21. Recovery initialization

The horizontal divisions are not to scale, they are a reference to show the sequence of operation. Either individual nPx_HS and Px_LS or nPx_Combined may be used. nPx_Combined is defined as both nPx_HS and Px_LS tied together or operated to the same logic level simultaneously.

7.3.3 IC initialization

This process flow initializes the IC and its software environment.

1. Apply power (V_{SYS}) to module
2. Remove $\overline{RST}$ ($\overline{RST}$ goes high, EN1 and EN2 are still low)
   2.1. When $\overline{RST}$ rises above the threshold, the device powers up. The charge pump (if configured) starts, allow V_{DD} and V_{LS} to stabilize.
3. Initialize registers
   3.1. Clear all interrupt status flags (send CINT0 and CINT1)
   3.2. Initialize MASK register by sending 0010 xxxx or 0011 xxxx to mask out unwanted interrupts.
   3.3. Set desired dead time either by commanding zero dead time or calibrating the dead time.
   3.4. Send MODE command with desired bits, and also the Lock bit. e.g. 01000001. This prevents further mode changes.
4. Bring EN1 and EN2 high
5. Initialize the outputs
   5.1. Command all $\overline{Px\_HS}$ to logic 1 (high-side OFF)
   5.2. Command all Px_LS to logic 1 (commanding low-side ON). The input must transition from low to high after EN1 and EN2 have gone high.
   5.3. Wait for the bootstrap capacitors to charge (about 1 us typically)
   5.4. Command all Px_LS to logic 0 (command low-side OFF)
   5.5. Command all $\overline{Px\_HS}$ to logic 0 (command high-side ON)
   5.6. Command all $\overline{Px\_HS}$ to logic 1 (command high-side OFF)

The device is now ready for normal operation.

7.3.4 Interrupt handler

When an interrupt occurs, the general procedure is to send NULL0 and NULL1 commands to determine what happened, take corrective action (if needed), clear the fault and return. Because the return value from an SPI command is actually returned in the subsequent message, main-loop software tries to read SR1, SR2, or SR3, may experience an interrupt between sending the SPI command and the subsequent read. Thus if these registers are to be read, special care must be taken in the software to ensure the correct results are being interpreted.

8 Typical applications

8.1 Typical 12 V application

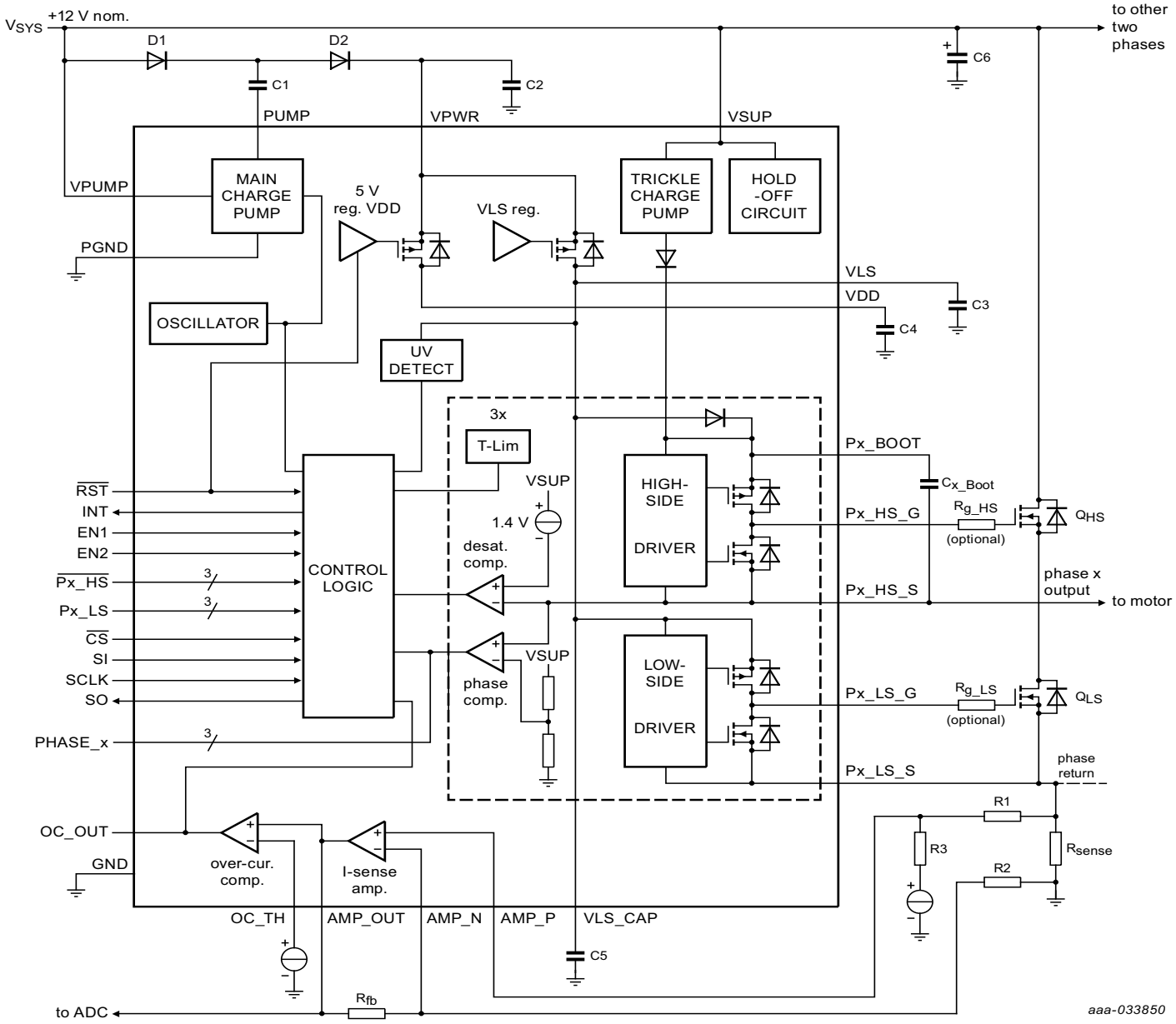


Figure 22. Typical 12 V application diagram using charge pump (+12 V battery system)

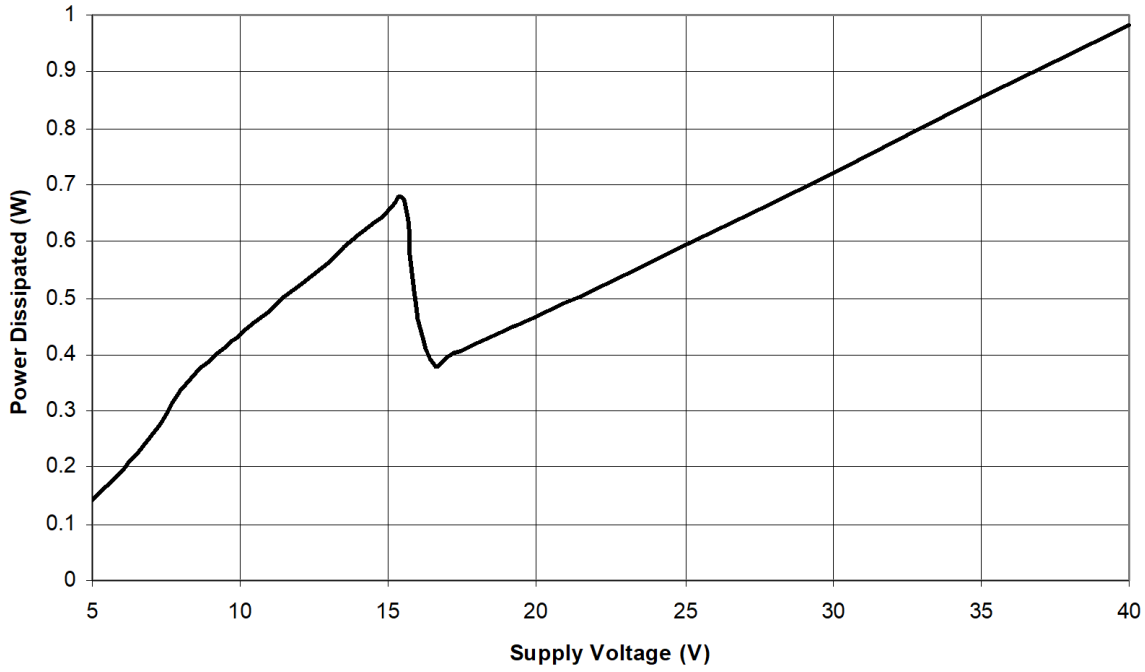


Figure 23. Power dissipation profile of application using charge pump

Reference application with:

- Pump capacitor: 1.0 μF MLC
- Pump filter capacitor: 47 μF low ESR aluminum electrolytic
- Pump diodes: MUR120
- Output FET gate charge: 240 nC @ 10 V
- PWM frequency: 20 kHz
- Switching single phase

Below approximately 17 V the charge pump is actively regulating V_{PWR}. The increased power dissipation is due to the charge pump losses. Above this voltage the charge pump oscillator shuts down and V_{SYS} is passed through the pump diodes directly to V_{PWR}.

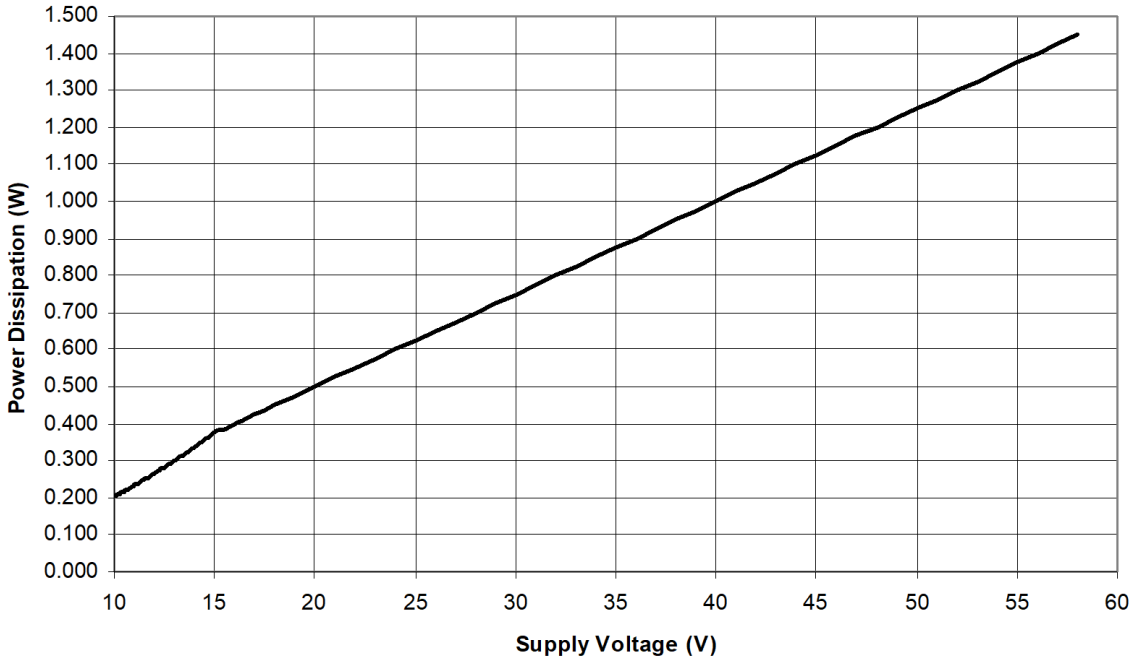


Figure 24. Power dissipation profile of application not using charge pump

Reference application with:

- Output FET gate charge: 240 nC @ 10 V
- PWM frequency: 20 kHz
- Switching single phase
- No connections to PUMP or VPUMP
- VPWR connected to V_{SYS}

If VPWR is supplied by a separate pre-regulator, the power dissipation profile is nearly flat at the value of the pre-regulator voltage for all V_{SYS} voltages.

8.2 Recommended 48 V application

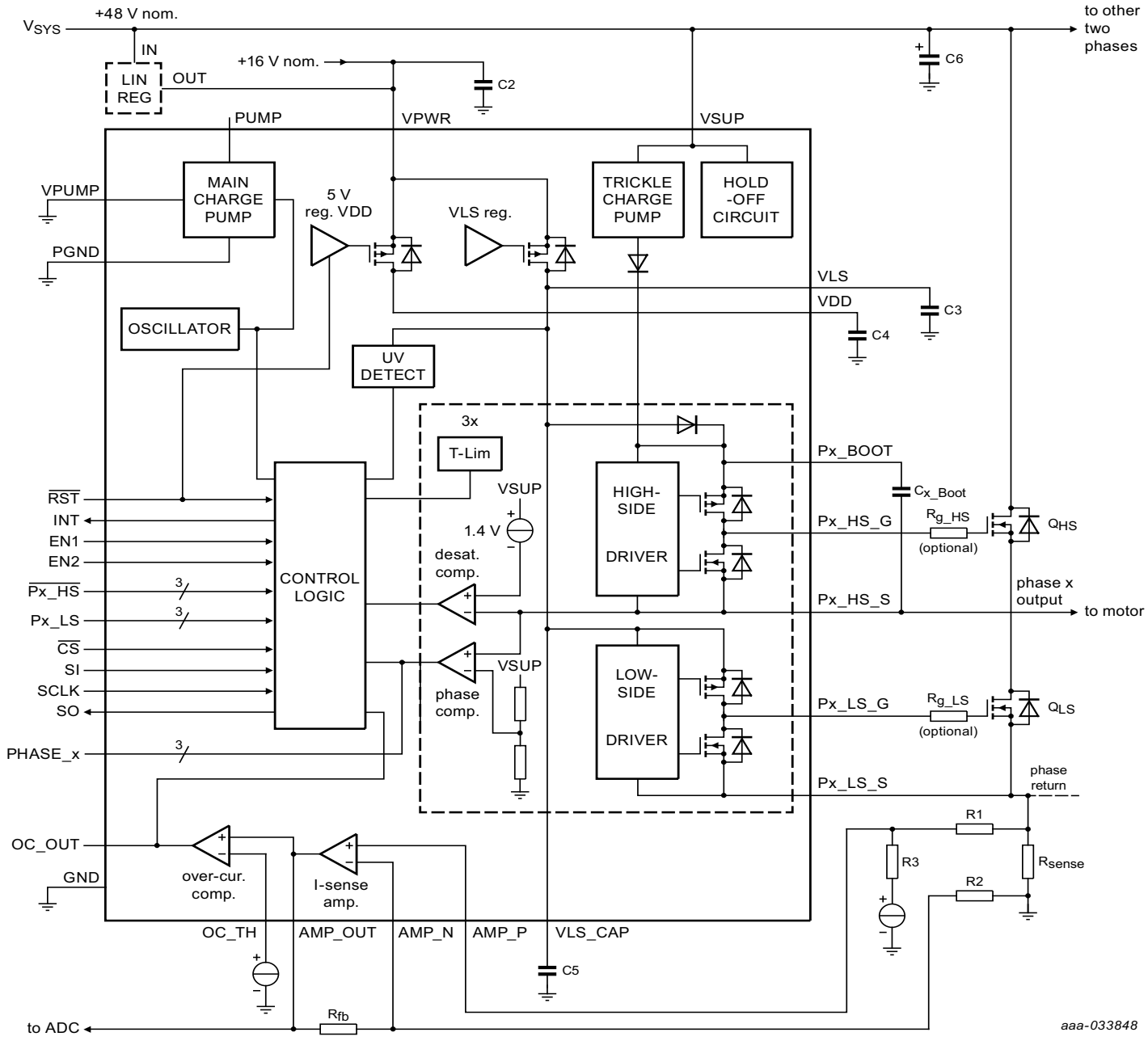


Figure 25. Recommended 48 V application diagram

9 Packaging

9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 20. Packaging information

Package	Suffix	Package outline drawing number
56-Pin QFN	EP	98ASA00654D

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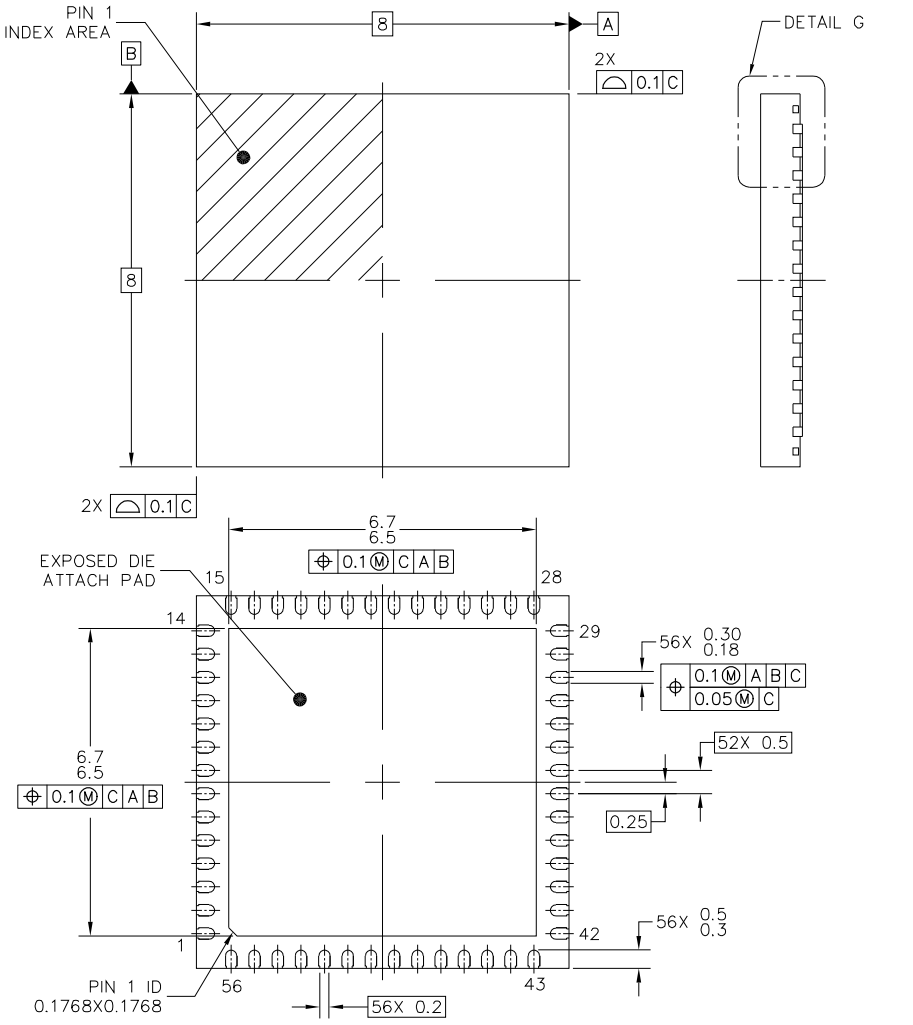

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	STANDARD: NON-JEDEC	
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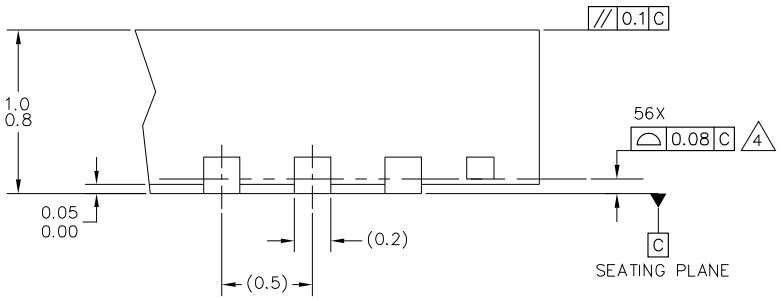

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
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	05 AUG 2014	

10 Revision history

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	4/2015	• Initial release
2.0	5/2015	• Updated thermal resistance value and unit in Table 3
	7/2015	• Changed part number from PC to MC in the Orderable parts on page 2
	8/2015	• Corrected Operating Junction Temperature value in Table 3
3.0	10/2015	• Revised V_{ESD} values in Table 3
4.0	12/2015	• Corrected upper end operating range value on page 1 • Corrected V_{SUP} value in Table 3
5.0	6/2018	• Updated targeted application on page 1
6.0	8/2018	• Added AEC-Q100 grade 1 qualified to general description and features list on page 1
7.0	4/2019	• Moved content from Section 8 to Section 8.1 • Added Section 8.2

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4/2019