PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8673
Dated 29 Aug 2014

ADDING GLOBAL FOUNDRIES WAFER FOUNDRY FOR MANUFACTURING BCD6/20-40V AND BCD6S/20V-40V TECHNOLOGY

Table 1. Change Implementation Schedule

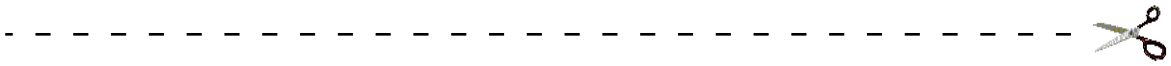
Forecasted implementation date for change	20-Nov-2014
Forecasted availability date of samples for customer	22-Aug-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	22-Aug-2014
Estimated date of changed product first shipment	28-Nov-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab additional location
Reason for change	to increase Advanced BCD technology manufacturing flexibility and capacity
Description of the change	ST is pursuing the plan to rationalize the manufacturing processes to increase flexibility and capacity. Because of this, ST is announcing that the wafer foundry Global Foundries located in Singapore, will be used to manufacture BCD6 technology based products actually manufactured in M5 Wafer fab, Catania, Italy. Wafer Fab Global Foundries has been already qualified by ST. This change will not affect EWS (Electrical Wafer Sort) activities and sites.
Change Product Identification	see new FG's
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8673**
Please sign and return to STMicroelectronics Sales Office	**Dated 29 Aug 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

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ADDING *GLOBAL FOUNDRIES* WAFER FOUNDRY FOR MANUFACTURING BCD6/20-40V AND BCD6S/20V-40V TECHNOLOGY

WHAT is the change?

ST is pursuing the plan to rationalize the manufacturing processes to increase flexibility and capacity. Because of this, ST is announcing that the wafer foundry Global Foundries located in Singapore, will be used to manufacture BCD6 technology based products actually manufactured in M5 Wafer fab, Catania, Italy.
Wafer Fab Global Foundries has been already qualified by ST. This change will not affect EWS (Electrical Wafer Sort) activities and sites.

Technology Family	Technology Sub family	Products line Codes	Package/ASSY SITES
BCD6	BCD6 40v	UM90	QFN/CARSEM PowerSO/ST MUAR
	BCD6 20V	UM85	QFN/CARSEM HSOP/AMKOR-FUJTSU
	BCD6 20V	UM87	QFN/CARSEM
BCD6S	BCD6S 20V	UA27	QFN/CARSEM SO8/ST SHENZHEN
	BCD6S 40V	UA28	QFN/CARSEM

WHY:

In order to increase Advanced BCD technology manufacturing flexibility and capacity.

WHEN will this change occur?

The added use of the Global Foundries capacity will start from Q4-2014 for the above mentioned products.

HOW will the change be qualified?

- This change will be qualified using the standard STMicroelectronics procedures for quality and reliability.
  Specific activities, included a full set of evaluations on selected test vehicles (TVs) will cover both : process qualification and product qualification. These include Wafer Level Reliability evaluation, Wafer Parametric comparison (T84), EWS comparison, Electrical characterization, die and package oriented reliability stress test.
  Other products manufactured with same technology will be qualified mainly by similarity (generic data).
  This transfer to Global Foundries will not modify the electrical, dimensional and thermal parameters for the product affected, keeping unchanged current description on relevant data sheets.

Qualification Program and results availability

See the attached Product Reliability Reports with the test done on the Test Vehicles (Product Reliability and ESD/LU on UA27). Qualification Reports for the other TVs will be available as by schedule.

Samples availability

Samples availability is: since wk34 for UA27, after wk34 for all others.

Change Implementation schedule

The production start and first shipments will be implemented according to the reported time line, as summarized below

Test Vehicles by Line codes	Product Family Code	Product family Description	PCN date	Qualification report availability	Forecasted First shipments
UA27	92	Power Conversion	WK34	WK34	WK46
UA28	I3	Hand Held PM	WK34	WK38	WK46
UM90	I3	Hand Held PM	WK34	WK38	WK50
UM85	92	Power Conversion	WK34	WK38	WK50
UM87	92	Power Conversion	WK34	WK38	WK50

Reliability Report

Front-End Qualification:

BCD6 diffused in GLOBAL FOUNDRY

TV: ST1S40IPUR-UA2701
VFDFPN 4X4X1.0 8L PITCH 0.8

General Information	
Product Line	UA2701
Product Description	3A DC step down switching regulator
P/N	ST1S40IPUR
Product Group	IPG
Product division	IPC Power Conversion
Package	VFDFPN 4X4X1.0 8L PITCH 0.8
Silicon Process technology	BCD6 SHRINK

Locations	
Wafer fab	Global Foundries Fab 2 + AMK6 8”
Assembly plant	CARSEM S
Reliability Lab	IPG Catania Reliability Lab
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	Jun-2014	10	Vito Gisabella Giuseppe Giacopello	Giovanni Presti	Final report
1.1	July-2014				ESD/LU test on UA27DDF version

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Front-End Qualification: BCD6 diffused in GLOBAL FOUNDRY.
TV1 : ST1S40IPUR – UA2701 – VFDFPN 4X4X1.0 8L Pitch 0.8

The complete evaluation plan includes three different TVs in order to cover the main technological fixtures:

- TV1: ST1S40IPUR – UA2701 – VFDFPN 4X4X1.0 8L Pitch 0.8
- TV2: LNBH25 – UA28 – QFN4X4
- TV3: LNBH23 – UM90 – PSSO24

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The ST1S40 device is an internally compensated 850 kHz fixed-frequency PWM synchronous stepdown regulator. The ST1S40 operates from 4.0 V to 18 V input, while it regulates an output voltage as low as 0.8 V and up to VIN. The ST1S40 integrates a 95 m□ high side switch and 69 m□ synchronous rectifier allowing very high efficiency with very low output voltages. The peak current mode control with internal compensation delivers a very compact solution with a minimum component count. The ST1S40 is available in HSOP-8, VFQFPN 4 mm x 4 mm - 8 lead, and standard SO8 package.

4.2 Construction note

	ST1S40IPUR
Wafer/Die fab. information	
Wafer fab manufacturing location	Global Foundries Fab 2+AMK6 8”
Technology	BCD6 SHRINK
Die finishing back side	Cr/NiV/Au
Die size	1725, 1840 micron
Passivation type	TEOS / SiN/Polymide
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ASL1K
Tester Program	UA27_ST1S40_rev2
Assembly information	
Assembly site	CARSEM S
Package description	VFDFPN 4X4X1.0 8L PITCH 0.8
Molding compound	Epoxy
Frame material	CDA 194 128X97 Mils Ni/Pd/Au
Die attach material	Epoxy
Wires bonding materials/diameters	1.3 mils Au wire
Final testing information	
Testing location	CARSEM S
Tester	ASL1K
Test program	UA27_ST1S40_CARSEM_rev6

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line	Comments
1	F2331222	SGC*ENGD4805,SG	MY3I*UA27DCF	VFDFPN 8L 4X4X1.0 PITCH 0.8	UA27	
2	F2330309	SGC*ENGD4905,S				
3	F2330310	ENGE04A1				

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS 1°LOT	2°LOT	3°LOT	Note
Die Oriented Tests									
HTOL	N	JESD22 A-108	Tj = 125°C Vin= +20V, Vfb= +2.5V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
E.L.F.R.	N	JESD22 A-108	Tj = 125°C, Vin= +20V, Vfb= +2.5V		48H		0/800		
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	Go no go
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/25	0/25	0/50	
					168 H	0/25	0/25	0/50	Eng. evaluation
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 CY	0/25	0/25	0/50	
					200 CY	0/25	0/25	0/50	
					500 CY	0/25	0/25	0/50	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, Vin= +16V, Vfb= +2V		168 H	0/25	0/25	0/50	
					500 H	0/25	0/25	0/50	
					1000 H	0/25	0/25	0/50	
Other Tests									
						UA27DCF	UA27DDF		
ESD	N	JEDEC JS001-2012 AEC Q101-002 and 005	HBM	3	+/-2KV	PASS	PASS		
			CDM	3	+/-500V	PASS	PASS		All Pins
				3	+/-750V	PASS	PASS		Corner Pin
			MM	3	+/-100V	PASS			
				3	+/-200V	PASS			
LU	N	EIA/JESD78D	CURRENT INJ. OVERVOLTAGE	6	+/- 100mA		PASS		

6 ANNEXES

6.1 Device details

6.1.1 Pin connection

Figure 2. Pin connection (top view)

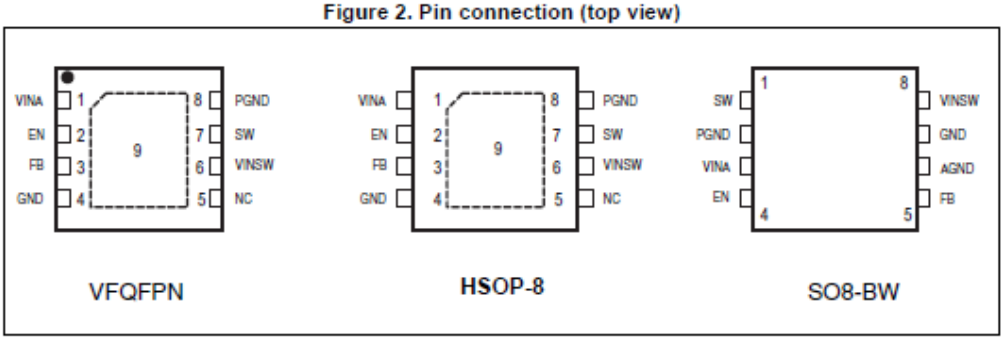
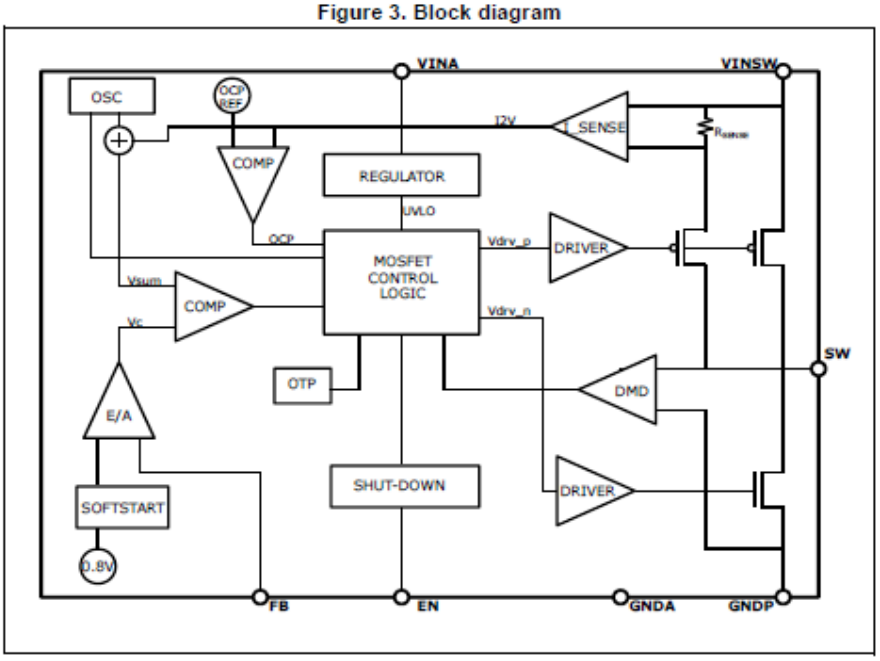


Table 1. Pin description

No.		Type	Description
VFQFPN and HSOP-8	S08-BW		
1	3	V_{INA}	Unregulated DC input voltage
2	4	EN	Enable input. With EN higher than 1.2 V the device in ON and with EN lower than 0.4 V the device is OFF (ST1S40Ixx).
3	5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8 V. To have higher regulated voltages an external resistor divider is required from Vout to the FB pin.
4	6	AGND	Ground
5	-	NC	It can be connected to ground
6	8	VINSW	Power input voltage
7	1	SW	Regulator output switching pin
8	2	PGND	Power ground
-	7		Ground
9	-	ePad	Exposed pad mandatory connected to ground

6.1.2 Block diagram

Figure 3. Block diagram



6.1.3 Package outline/Mechanical data

Figure 19. VFQFPN8 (4 x 4 x 1.0 mm) package outline

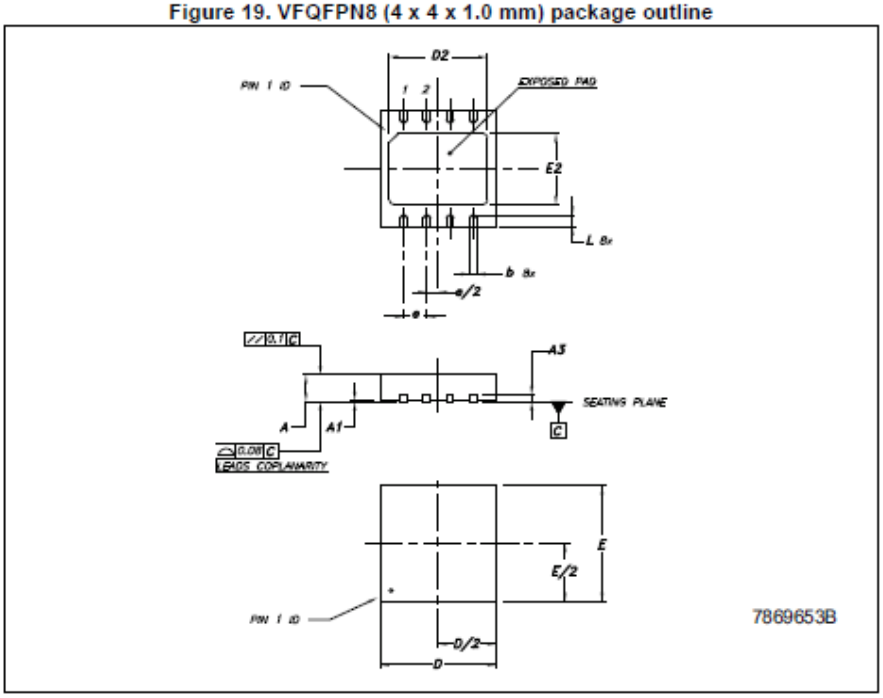


Table 10. VFQFPN8 (4 x 4 x 1.0 mm) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.23	0.30	0.38	0.009	0.0117	0.0149
D	3.90	4.00	4.10	0.153	0.157	0.161
D2	2.82	3.00	3.23	0.111	0.118	0.127
E	3.90	4.00	4.10	0.153	0.157	0.161
E2	2.05	2.20	2.30	0.081	0.087	0.091
e		0.80			0.031	
L	0.40	0.50	0.60	0.016	0.020	0.024

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
ELFR Early Life Failure Rate	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	The objective of ELFR is to measure the failure rate in the first several months or year of operation.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM:** Charged Device Model **HBM:** Human Body Model **MM:** Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up

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