


PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.	IPD/15/9179	
1.3 Title of PCN	L4984D (Product Line UE41) : Metal mask modification	
1.4 Product Category	L4984D and L4984DTR (CCM PFC controller)	
1.5 Issue date	2015-04-27	

2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Francesca Marta SANDRINI
2.1.2 Marketing Manager	Vincenzo MONTEMEZZO
2.1.3 Quality Manager	Paolo MORETTI

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Die redesign	Functional / pin layout change	Ang Mo Klo, Singapore

4. Description of change

	Old	New
4.1 Description	Current silicon version is UE41AC6	New silicon version is UE41AD6
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change

5.1 Motivation	For designs that do not use a Start up network with external mosfet, there could be a potential risk of misbehavior of the device. In order to prevent this problem, the UVLO block has been changed so as to provide a stable Supply Current before Start up from zero to the Vcc Turn-on threshold.
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change

6.1 Description	This modification will be identified by a new internal part number : L4984D-3/ L4984DTR-3/
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7. Timing / schedule

7.1 Date of qualification results	2015-04-01
7.2 Intended start of delivery	2015-10-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	UE41 Reliability Report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2015-04-27

9. Attachments (additional documentations)

9179PpPrdtLst.pdf
UE41 Reliability Report.pdf
L4984D-3 VERIFICATION BY APPLICATION TEAM.pdf

10. Affected parts

10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	L4984DTR	

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Public Products List

PCN Title : L4984D (Product Line UE41) : Metal mask modification

PCN Reference : IPD/15/9179

PCN Created on : 01-Apr-2015

Subject : Public Product List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

L4984DTR	L4984D	
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23/Febr./2015 Plastic sample, soldered on EVL4984-350W ST demo-board

Ton time evaluation

After a test on a sample of the previous silicon version to have a reference image (Image 1), tests have been performed on a sample of the new silicon version at different supply voltage and temperature. All the tests have been performed with $C_{VCC} = 100 \mu\text{F} + 470 \text{ nF}$

and $R_{\text{startup}} = 300 \text{ k}\Omega$

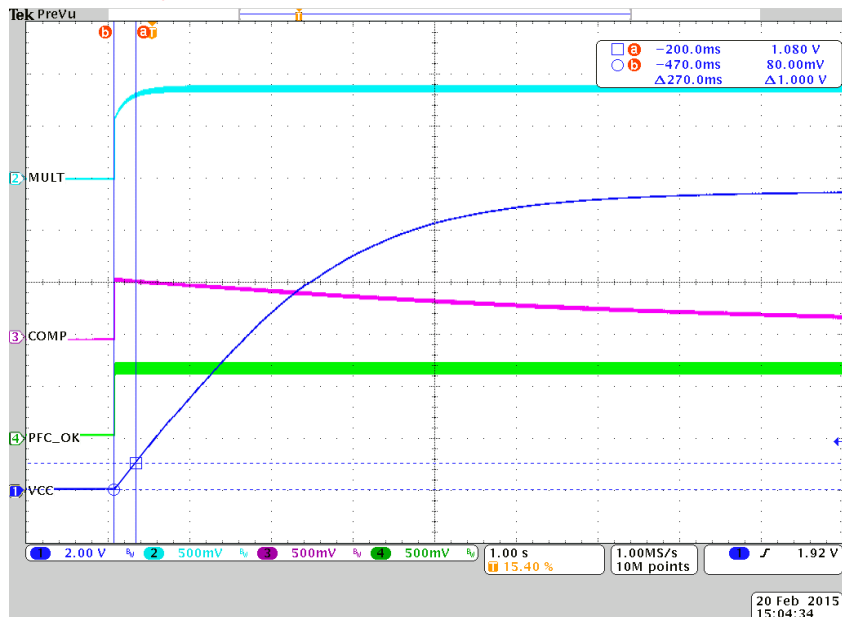
The behavior of the sample was correct. For some images see from 2 to 7 .

1

INCORRECT BEHAVIOR OF THE PREVIOUS SILICON

L4984D -

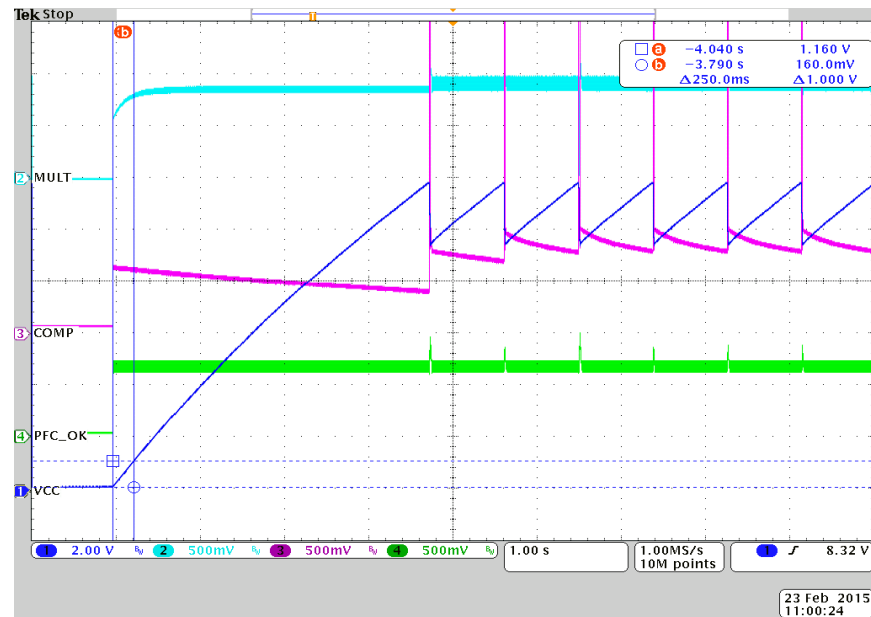
T=ambient, Vac=90 V - 60 Hz



2

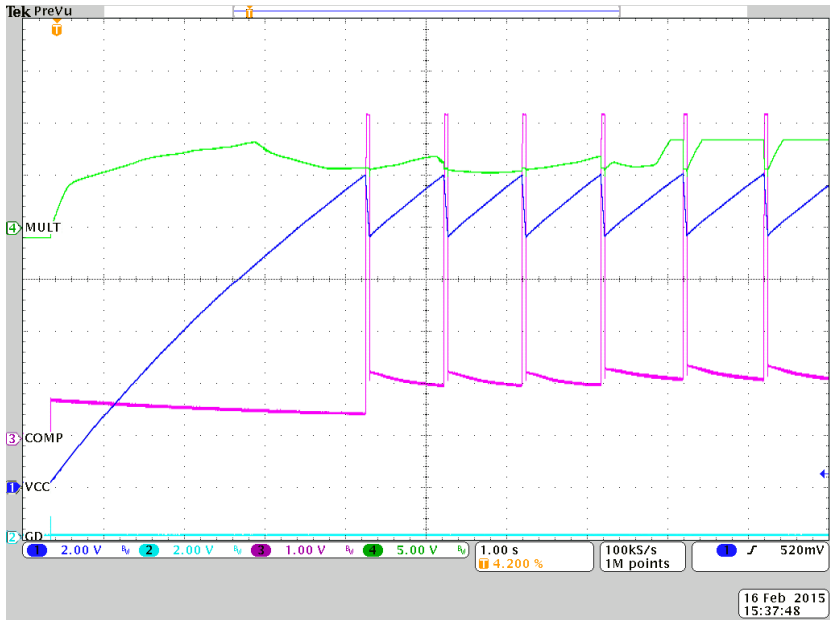
L4984D NEW

T=ambient, Vac=90 V - 60 Hz



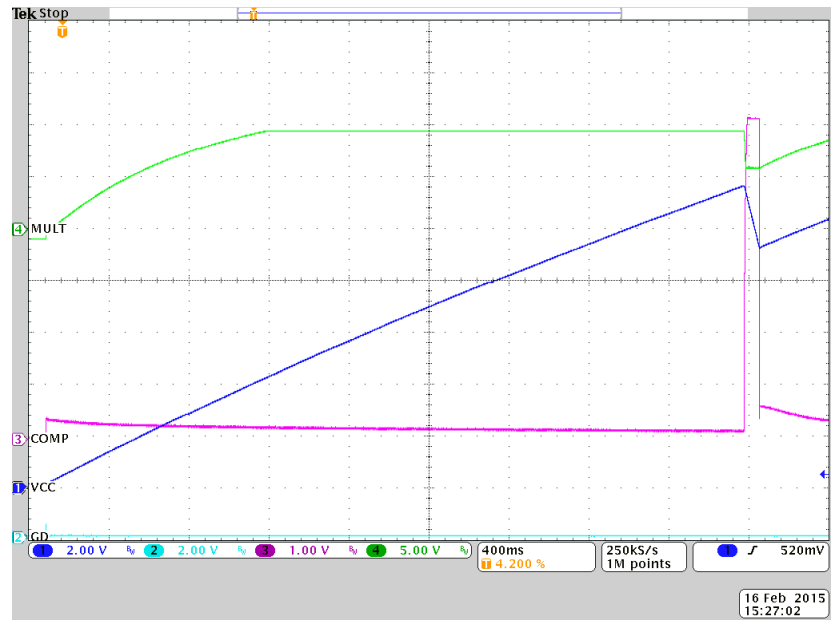
3

L4984D NEW
T=high*, Vac=90 V - 60 Hz



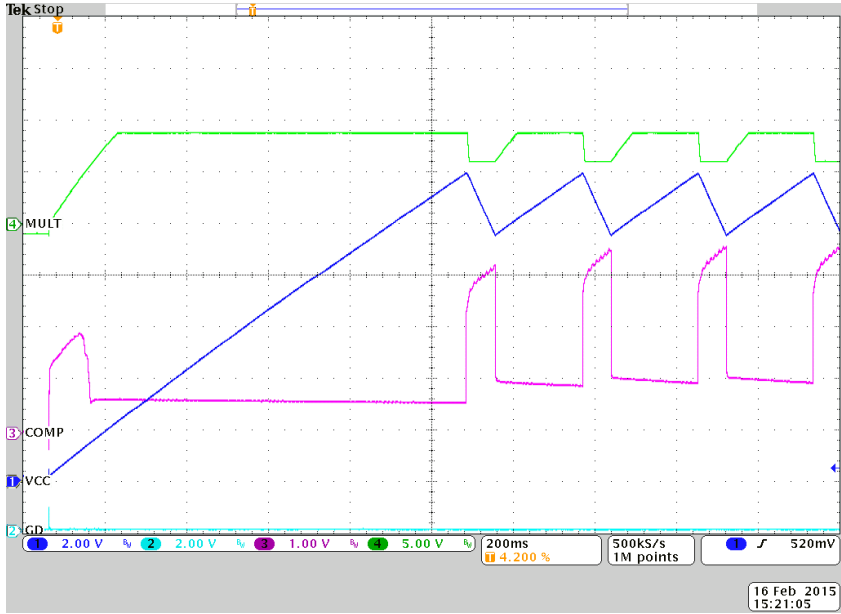
4

L4984D NEW
T=low*, Vac=90 V - 60 Hz



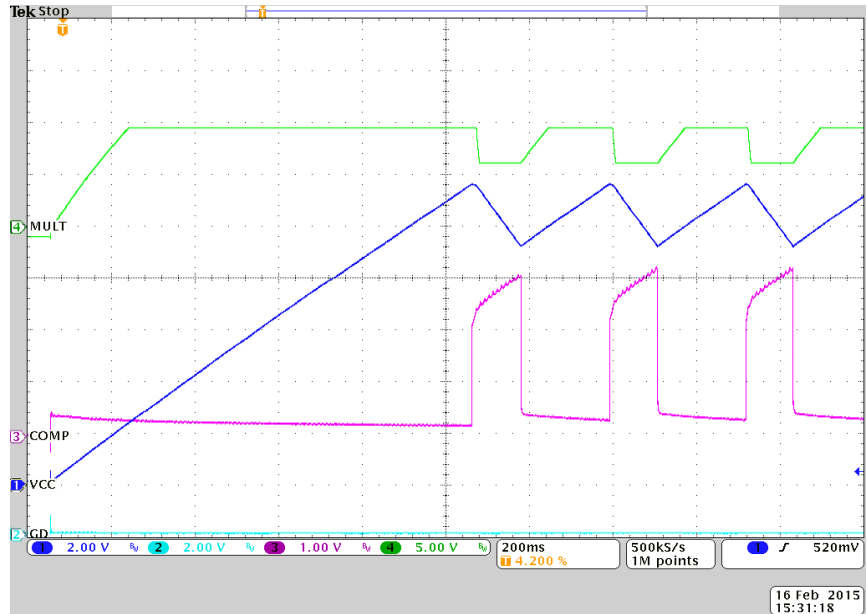
5

L4984D NEW
T=ambient, Vac=264 V - 50 Hz



6

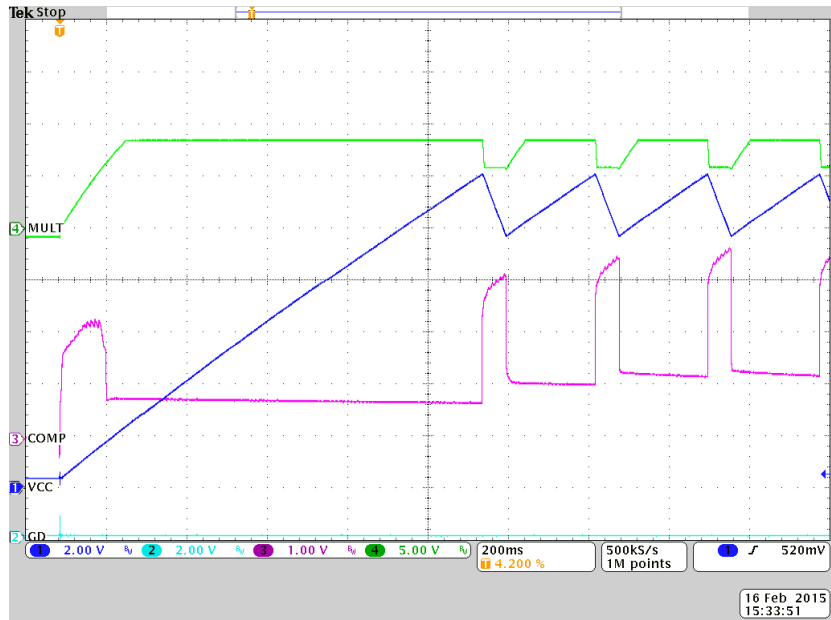
L4984D NEW
T=high*, Vac=264 V - 50 Hz



7

L4984D NEW

T=low*, Vac=264 V - 50 Hz



23/Febr./2015 Plastic sample, soldered on EVL4984-350W ST demo-board

Dependence of Tstart (startup time) from temperature and Vac supply voltage

* Thigh: the samples was heated by a hot-air gun setted at 160 C for 2 minutes

*Tlow: the samples was cooled down by a spray can

Reliability Report

General Information	
Product Line	<i>UE41</i>
Product Description	<i>CCM PFC CONTROLLER</i>
Product division	<i>I&PC</i>
Package	<i>SSOP 10L</i>
Silicon process technology	<i>BCD2S</i>

Locations	
Wafer fab location	<i>ANG MO KIO</i>
Assembly plant location	<i>BOUSKOURA</i>
Reliability assessment	<i>Pass</i>

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	21-Apr-15	13	S.O.Cannizzaro	Original document

Approved by

Alceo Paratore

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of the UE41 device diffused in ANG MO KIO and assembled in SSOP 10L in BOUSKOURA.

According to Reliability Qualification Plan, below is the list of the trials performed:

Package Oriented Tests

- Preconditioning
- Temperature Cycling
- Autoclave
- High Temperature Storage Life
- Thermal Humidity Storage

Electrical Characterization

- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the trials performed the UE41 diffused in ANG MO KIO and assembled in SSOP 10L in BOUSKOURA **can be qualified** from reliability viewpoint.

3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Generalities

The device is a current-mode PFC controller operating with line-modulated fixed-off-time (LMFOT) control. A proprietary LM-FOT modulator allows fixed-frequency operation for boost PFC converters as long as they are operated in CCM (Continuous Conduction Mode).

The chip comes in a 10 pin SO package and offers a low-cost solution for CCM-operated boost PFC pre-regulators in EN61000-3-2 and JEIDAMITI compliant applications, in a power range that spans from few hundred W to 1 kW and above.

The highly linear multiplier includes a special circuit, able to reduce the crossover distortion of the ac input current, that allows wide-range-mains operation with a reasonably low THD, even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @T_j = 25°C) internal voltage reference.

Loop stability is optimized by the voltage feedforward function (1/V₂ correction), which in this IC uses a proprietary technique that significantly improves also line transient response in case of mains drops and surges ("bidirectional").

The device features low consumption and includes a disable function suitable for IC remote ON/OFF. These features allow the usage in applications supposed to comply even with the latest energy saving requirements (Blue Angel, EnergyStar, Energy2000, etc.).

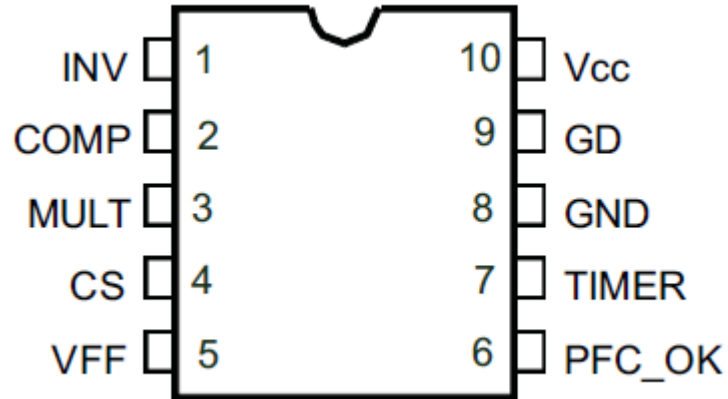
In addition to an over voltage protection able to keep the output voltage under control during transient conditions, the IC is provided also with a protection against feedback loop failures or erroneous settings.

Other on-board protection functions allow that brownout conditions and boost inductor saturation can be safely handled.

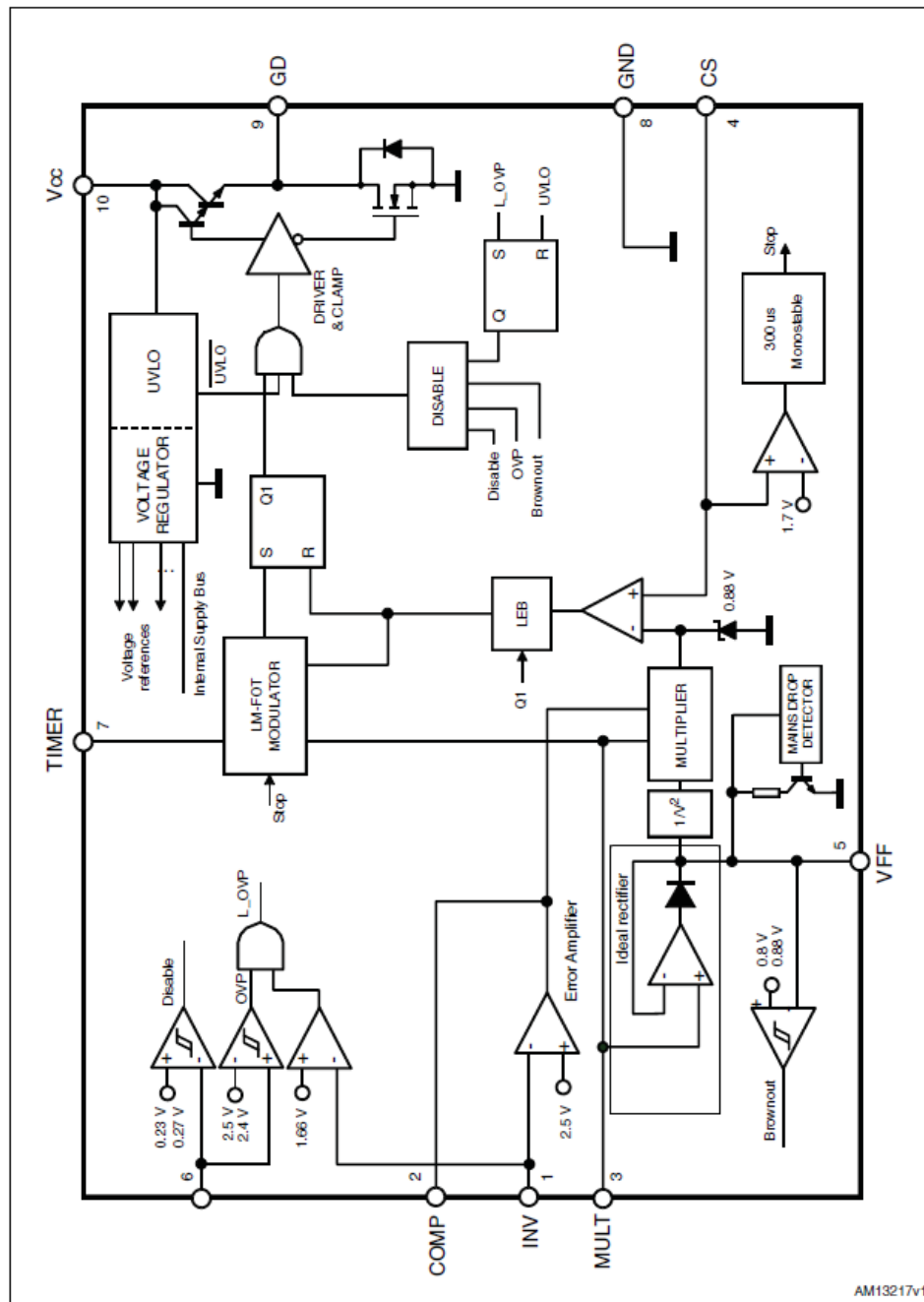
Soft-start limits peak current and extends OFF time to prevent flux runaway in the initial cycles.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOSFET or IGBT drive.

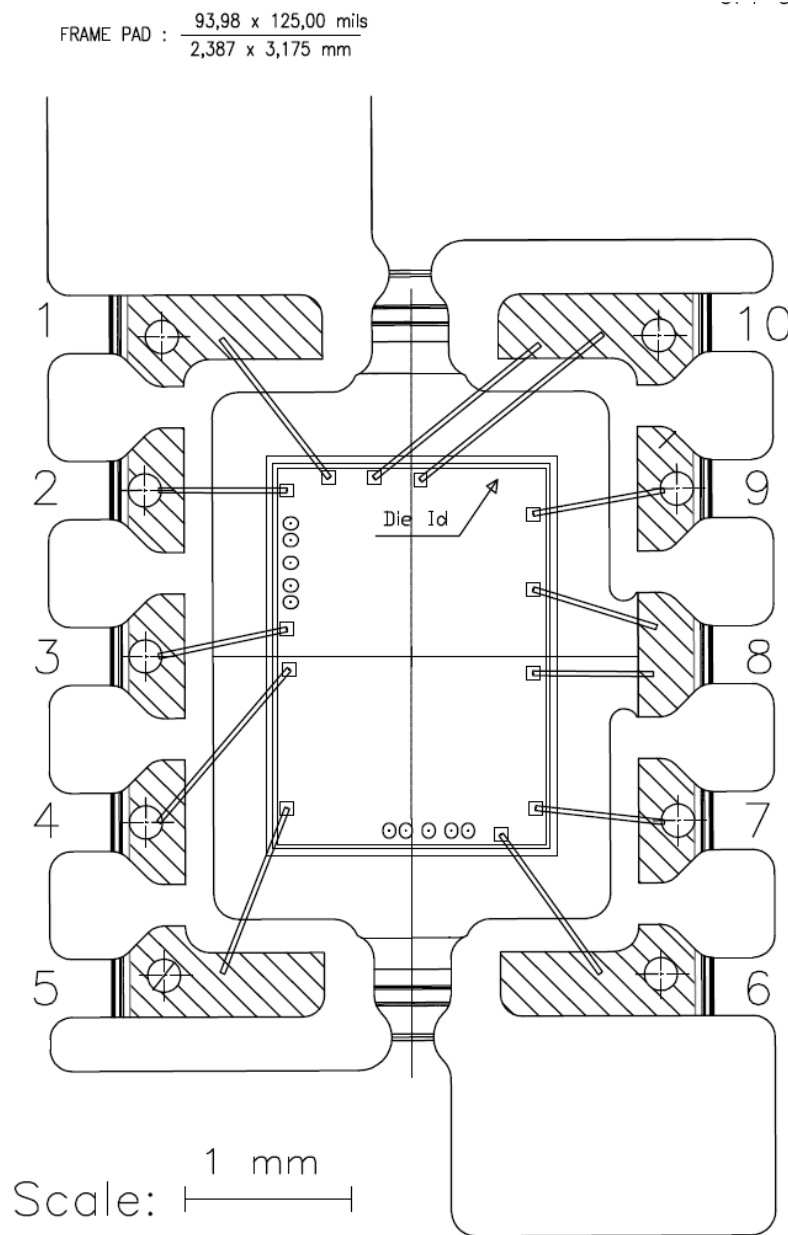
3.1.2 Pin connection



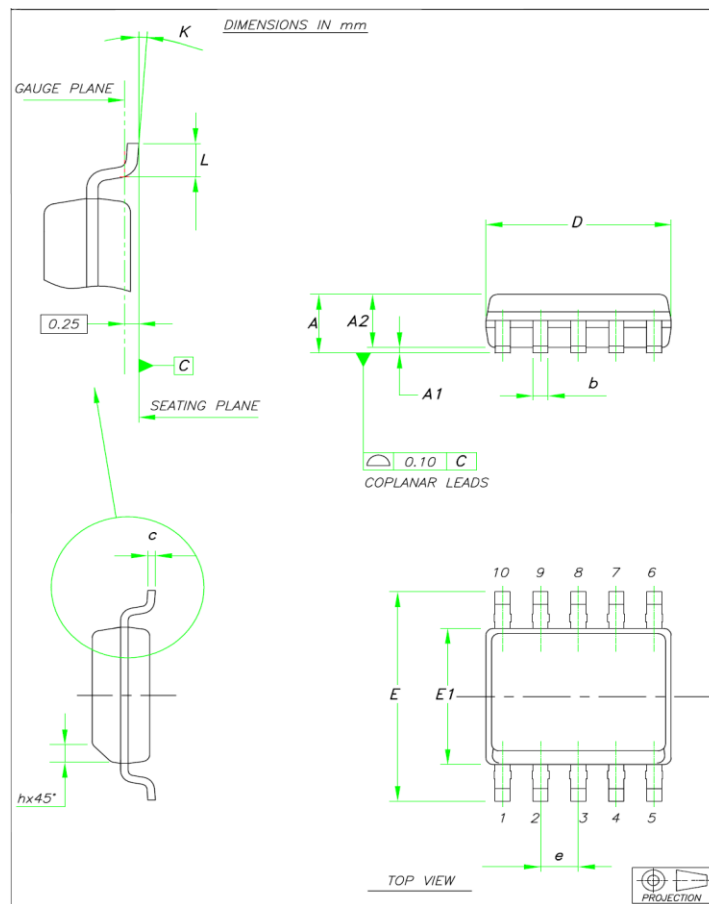
3.1.3 Block diagram



3.1.4 Bonding diagram



3.1.5 Package outline/Mechanical data



3.2 Traceability

Wafer fab information	
Wafer fab manufacturing location	ANG MO KIO
Wafer diameter	6 inches
Wafer thickness	375 μ m
Silicon process technology	BCD2S
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size	1770x2430 μ m
Bond pad metallization layers	AlSiCu
Passivation	NITRIDE
Metal levels	2

Assembly Information	
Assembly plant location	BOUSKOURA
Package description	SSOP 10L
Molding compound	G700K
Wires bonding materials/diameters	Au/1mils
Die attach material	8601S-25
Lead solder material	NiPdAu

4 TESTS RESULTS SUMMARY

4.1 LOTs information

Lot ID #	Comments
Lot 1	UE41 ¹²
Lot 2	UE40

4.2 Test plan and results summary

Package Oriented Tests						
Test	Method	Conditions	Failure/SS		Duration	Note
			Lot 1	Lot 2		
PC	Pre-Conditioning: Moisture sensitivity level 3					
		192h 30°C/60% - 3 reflow PBT 260°C	0/77	0/250		
TC	Temperature Cycling					
	PC before	Temp. range: -65/+150°C	0/77	0/77	500cy	
AC	Autoclave					
	PC before	121°C 2atm	--	0/77	168h	
HTSL	High Temperature Storage					
	No bias	Tamb=150°C	--	0/77	1000h	
THS	Temperature Humidity Storage					
	No Bias	85%RH/85°C	--	0/77	1000h	

Electrical Characterization Tests						
Test	Method	Conditions	Failure/SS		Duration	Note
			Lot 1			
ESD	Electro Static Discharge					
	Human Body Model	+/- 1.5kV on Pin 5 +/- 2kV on other pins	0/3			
	Machine Model	+/- 200V	0/3			
	Charge Device Model	+/- 500V +/- 750V on corner pins	0/3			
LU	Latch-Up					
	Over-voltage and Current Injection	Tamb=85°C Jedec78	0/6			

¹ UE41 is a modification of the already qualified UE40.

² Trials on UE41 were performed on AC6 revision.

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Package oriented tests

5.1.1 Pre-Conditioning

The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.

The scope is to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

5.1.2 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.

The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.1.3 Temperature Humidity Storage

The device is stored in unbiased condition, at controlled conditions of ambient temperature and relative humidity. The scope is to investigate the failure mechanisms activated in the die-package environment in wet conditions.

5.1.4 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 200 cycles.
- Final Testing @ 500 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -65°C to +150°C(air)

5.1.5 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.

Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

5.2 Electrical Characterization Tests

5.2.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up. The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
<i>IN low: 0V</i>	-100mA Note1	Inom+100mA Note3	Vcc=22.5V
<i>IN high: 1.8V</i>	-100mA Note2	Inom+100mA Note3	Vcc=22.5V

Note1: Trigger voltage clamped at -0.7V (pins 4, 7, 2).

Note2: Trigger voltage clamped at -0.7V (pin 7), -0.2V (pin 4), -0.6V (pin 9).

Note3: Trigger voltage clamped at +2.4V (pin 4), +3.5V (pin 5, 7), +7V (pin 2), +16V (pin 9), +3.26 (pins 1, 3, 6)

5.2.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.

The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** ANSI/ESDA/JEDEC STANDARD JES001
- **Machine Model** JEDEC STANDARD EIA/JESD22-A115
- **Charge Device Model** ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101