OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ISL22416

ISL22419

Single Digitally Controlled Potentiometer (XDCP™) Low Noise, Low Power, SPI® Bus, 128 Taps, Wiper Only

FN6311
Rev 1.00
September 8, 2009

The ISL22419 integrates a single digitally controlled potentiometer (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the SPI serial interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up the device recalls the content of the DCP's IVR to the WR.

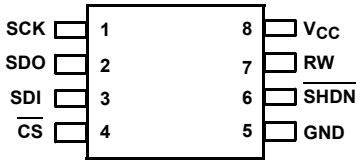
The DCP can be used as a voltage divider in a wide variety of applications including control, parameter adjustments, AC measurement and signal processing.

Features

- 128 resistor taps
- SPI serial interface
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ 3.3V
- Shutdown mode
- Shutdown current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- 8 Lead MSOP
- Pb-free (RoHS compliant)

Pinout

ISL22419
(8 LD MSOP)
TOP VIEW



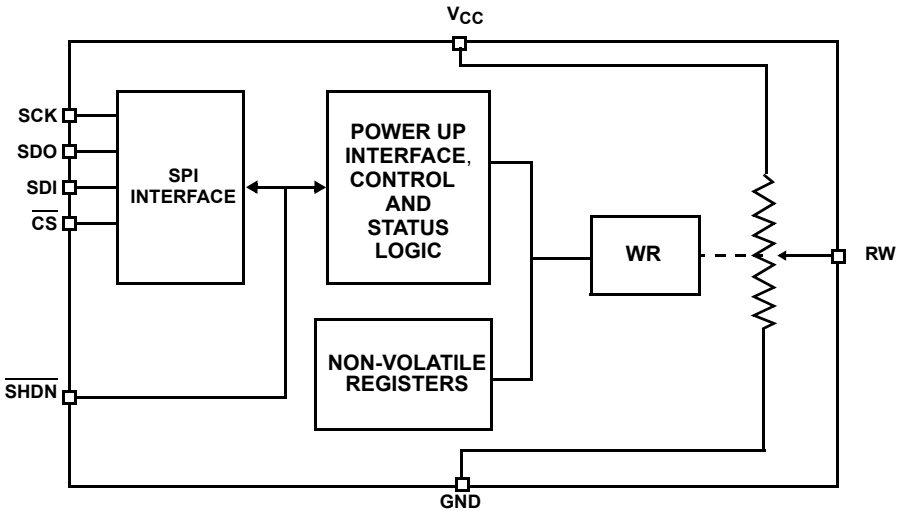
Ordering Information

PART NUMBER	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL22419UFU8Z*	419UZ	50	-40 to +125	8 Ld MSOP	M8.118
ISL22419WFU8Z*	419WZ	10	-40 to +125	8 Ld MSOP	M8.118

*Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

MSOP PIN	SYMBOL	DESCRIPTION
1	SCK	SPI interface clock input
2	SDO	Open Drain Data Output of the SPI serial interface
3	SDI	Data Input of the SPI serial interface
4	$\overline{CS}$	Chip Select active low input
5	GND	Device ground pin
6	$\overline{SHDN}$	Shutdown active low input
7	RW	“Wper” terminal of DCP
8	V_{CC}	Power supply pin

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to V_{CC} + 0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP pin with Respect to GND . . . . . -0.3V to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup (Note 2) . . . . . Class II, Level B @+125°C
ESD Rating
HBM 5kV
CDM) 1kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Lead MSOP	165

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature . . . . . -40°C to +125°C
V_{CC} Voltage for DCP Operation . . . . . 2.7V to 5.5V
Wiper Current . . . . . -3mA to 3mA
Power Rating 5mW

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -1V for all pins.

Analog Specifications — Over recommended operating conditions unless otherwise stated. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 3)	MAX	UNIT
R_{TOTAL}	End-to-End Resistance	W option		10		kΩ
		U option		50		kΩ
	End-to-End Resistance Tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±50		ppm/°C (Note 11)
		U option		±80		ppm/°C (Note 11)
R_W (Note 11)	Wiper Resistance	V_{CC} = 3.3V @ +25°C, wiper current = V_{CC}/R_{TOTAL}		70		Ω
C_W (Note 11)	Wiper Capacitance			25		pF
I_{LkgRW}	Leakage on RW Pin	Voltage at pin from GND to V_{CC}		2	4	µA
VOLTAGE DIVIDER MODE (measured at R_W, unloaded)						
INL (Note 7)	Integral Non-linearity		-1		1	LSB (Note 4)
DNL (Note 6)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 4)
ZSerror (Note 5)	Zero-scale Error	W option	0	1	5	LSB (Note 4)
		U option	0	0.5	2	LSB (Note 4)
FSerror (Note 6)	Full-scale Error	W option	-5	-1	0	LSB (Note 4)
		U option	-2	-1	0	LSB (Note 4)
TC_V (Notes 8, 11)	Ratiometric Temperature Coefficient	DCP register set to 40 hex		±4		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 3)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	10k DCP, f_{SPI} = 5MHz; (for SPI active, read and write states)			1	mA
	V_{CC} Supply Current (volatile write/read)	50k DCP, f_{SPI} = 5MHz; (for SPI active, read and write states)			0.5	mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	10k DCP, f_{SPI} = 5MHz; (for SPI active, read and write states)			3.2	mA
	V_{CC} Supply Current (non-volatile write/read)	50k DCP, f_{SPI} = 5MHz; (for SPI active, read and write states)			2.7	mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V, 10k DCP, SPI interface in standby state			850	µA
		V_{CC} = +5.5V, 50k DCP, SPI interface in standby state			160	µA
		V_{CC} = +3.6V, 10k DCP, SPI interface in standby state			550	µA
		V_{CC} = +3.6V, 50k DCP, SPI interface in standby state			100	µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V @ +85°C, SPI interface in standby state			3	µA
		V_{CC} = +5.5V@ +125°C, SPI interface in standby state			5	µA
		V_{CC} = +3.6V @ +85°C, SPI interface in standby state			2	µA
		V_{CC} = +3.6V @ +125°C, SPI interface in standby state			4	µA
I_{LkgDig}	Leakage Current, at Pins $\overline{SHDN}$, SCK, SDI, SDO and $\overline{CS}$	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{WRT} (Note 11)	Wiper Response Time	Wiper Response Time after SPI write to WR register		1.5		µs
$t_{ShdnRec}$ (Note 11)	DCP Recall Time from Shutdown Mode	From rising edge of $\overline{SHDN}$ signal to wiper stored position and RH connection		1.5		µs
		SCK rising edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	2.0		2.6	V
V_{CC} Ramp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and SPI Interface in standby state			3	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55°C	50			Years
t_{WC} (Note 9)	Non-volatile Write Cycle Time	From rising edge of $\overline{CS}$		12	20	ms
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	$\overline{SHDN}$, SCK, SDI, and $\overline{CS}$ Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V

Operating Specifications Over the recommended operating conditions unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

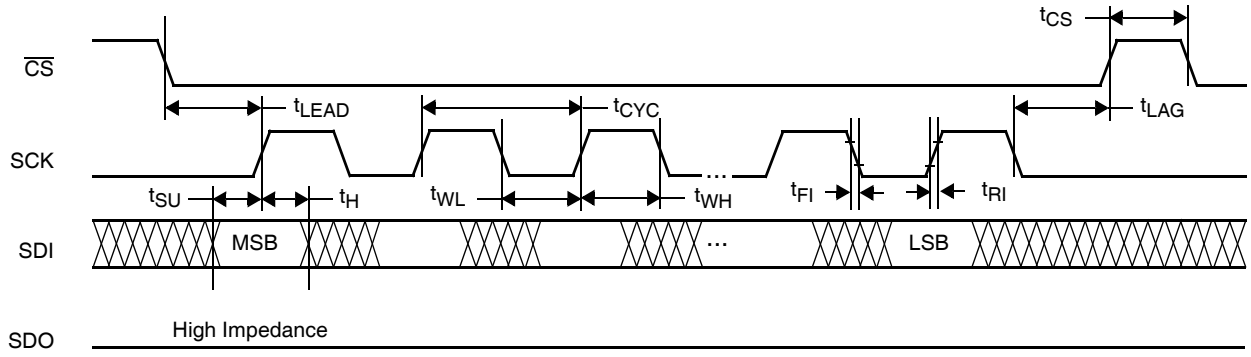
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 3)	MAX	UNIT
V_{IH}	$\overline{SHDN}$, SCK, SDI, and $\overline{CS}$ Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+0.3	V
Hysteresis	$\overline{SHDN}$, SCK, SDI, and $\overline{CS}$ Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL}	SDO Output Buffer LOW Voltage	I_{OL} = 4mA	0		0.4	V
R_{pu} (Note 10)	SDO Pull-up Resistor Off-chip	Maximum is determined by t_{RO} and t_{FO} with maximum bus load Cbus = 30pF, f_{SCK} = 5MHz			2	kΩ
Cpin (Note 11)	$\overline{SHDN}$, SCK, SDI, SDO and $\overline{CS}$ Pin Capacitance				10	pF
f_{SCK}	SPI Frequency				5	MHz
t_{CYC}	SPI Clock Cycle Time		200			ns
t_{WH}	SPI Clock High Time		100			ns
t_{WL}	SPI Clock Low Time		100			ns
t_{LEAD}	Lead Time		250			ns
t_{LAG}	Lag Time		250			ns
t_{SU}	SDI, SCK and $\overline{CS}$ Input Setup Time		50			ns
t_H	SDI, SCK and $\overline{CS}$ Input Hold Time		50			ns
t_{RI}	SDI, SCK and $\overline{CS}$ Input Rise Time		10			ns
t_{FI}	SDI, SCK and $\overline{CS}$ Input Fall Time		10		20	ns
t_{DIS}	SDO Output Disable Time		0		100	ns
t_V	SDO Output Valid Time				350	ns
t_{HO}	SDO Output Hold Time		0			ns
t_{RO}	SDO Output Rise Time	R_{pu} = 2k, Cbus = 30pF			60	ns
t_{FO}	SDO Output Fall Time	R_{pu} = 2k, Cbus = 30pF			60	ns
t_{CS}	CS Deselect Time		2			µs

NOTES:

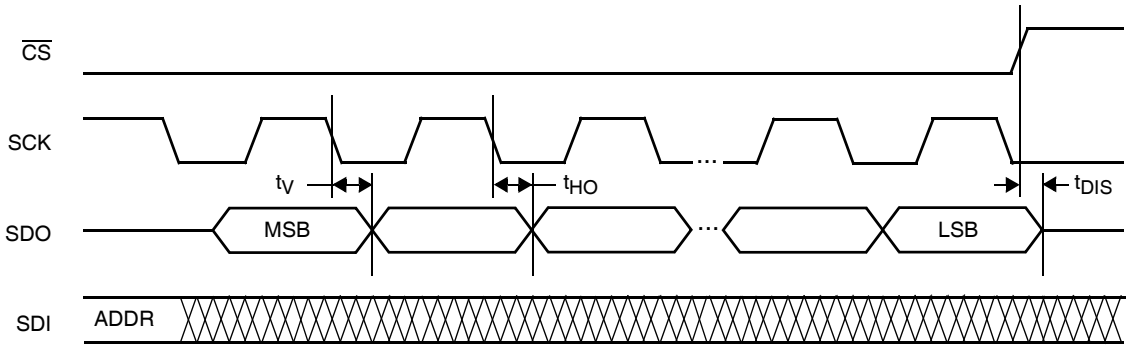
3. Typical values are for T_A = +25°C and 3.3V supply voltage.
4. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
5. ZS error = $V(RW)_0$/LSB.
6. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
7. INL = $[V(RW)_i – (i • LSB) – V(RW)_0]$/LSB for i = 1 to 127
8. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{165°C}$ for i = 16 to 127 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
9. t_{WC} is the time from the end of a Write sequence of SPI serial interface, to the end of the self-timed internal non-volatile write cycle.
10. R_{pu} is specified for the highest data rate transfer for the device. Higher value pullup can be used at lower data rates.
11. This parameter is not 100% tested.

Timing Diagrams

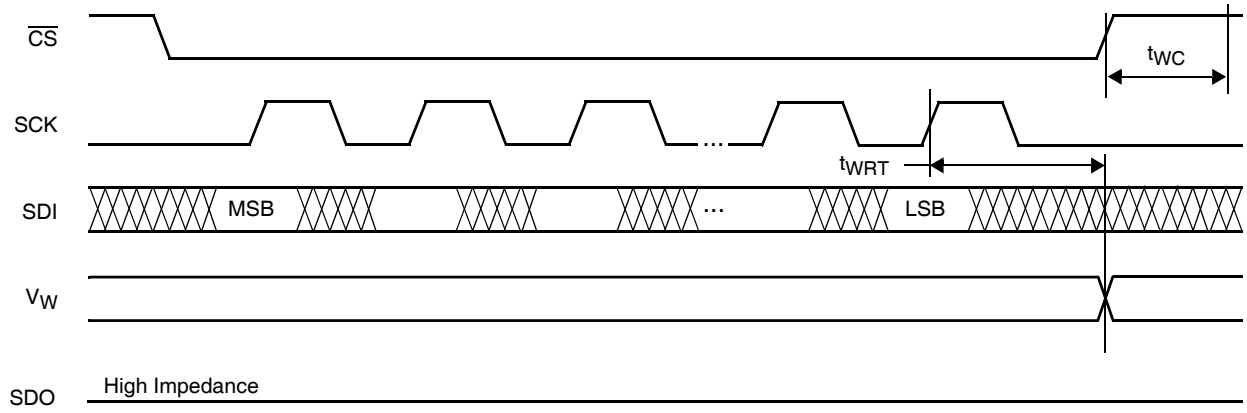
Input Timing



Output Timing



XDCP Timing (for All Load Instructions)



Typical Performance Curves

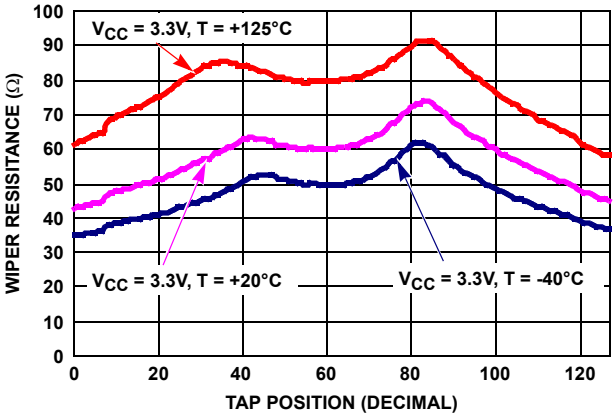


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

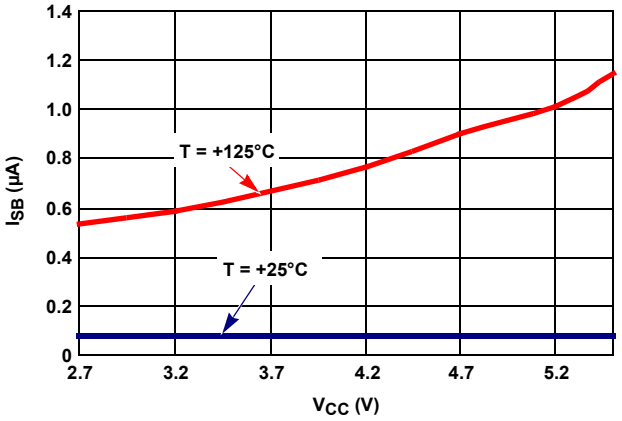


FIGURE 2. STANDBY I_{CC} vs V_{CC}

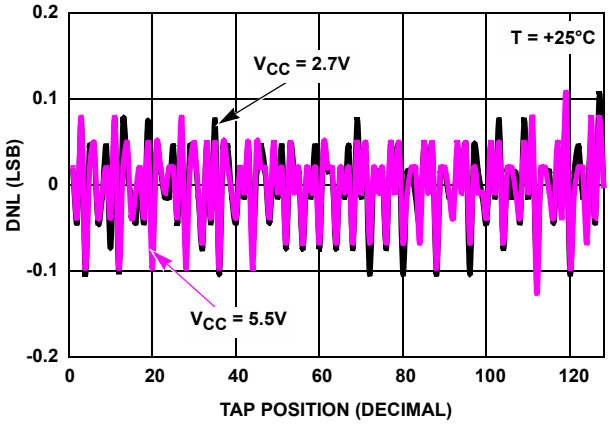


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

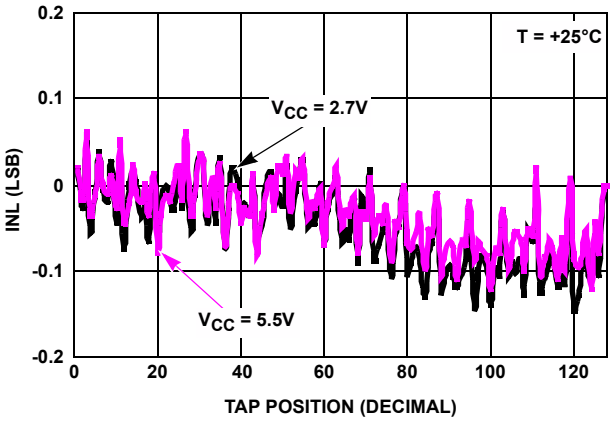


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

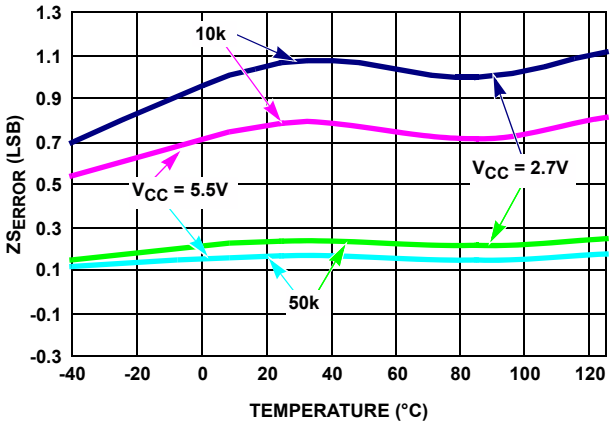


FIGURE 5. ZS_{ERROR} vs TEMPERATURE

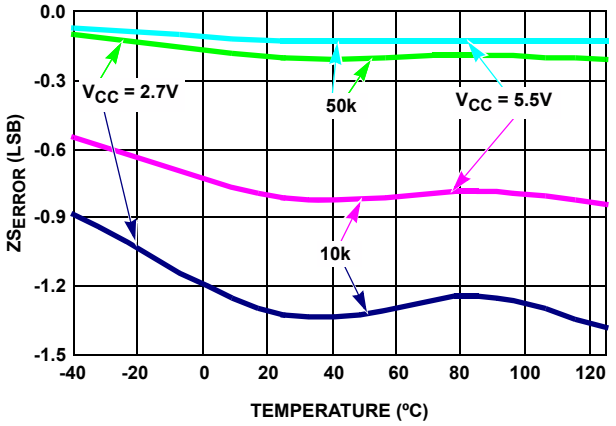


FIGURE 6. ZS_{ERROR} vs TEMPERATURE

Typical Performance Curves (Continued)

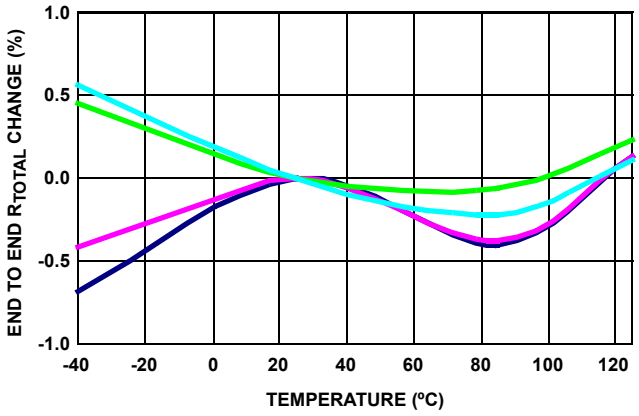


FIGURE 7. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

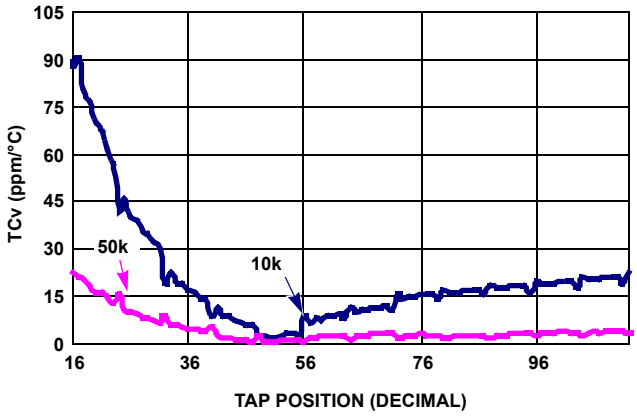


FIGURE 8. TC FOR VOLTAGE DIVIDER MODE IN ppm

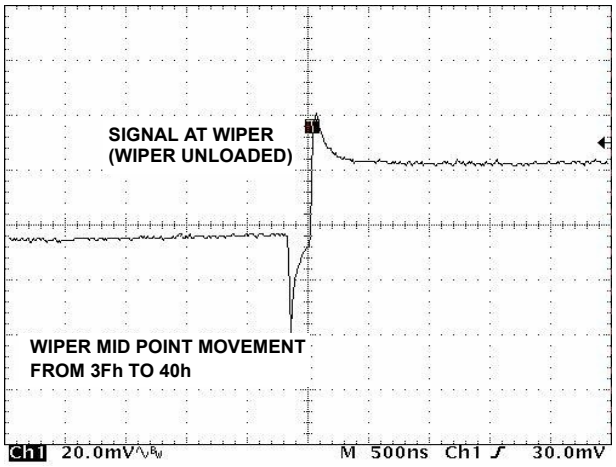


FIGURE 9. MIDSCALE GLITCH, CODE 80h TO 7Fh

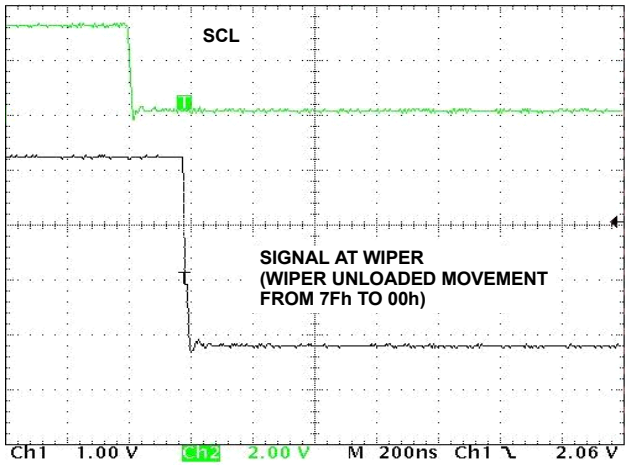


FIGURE 10. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometer Pins

RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

$\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin forces the resistor to end-to-end open circuit condition and shorts RW to GND. When $\overline{\text{SHDN}}$ is returned to logic high, the previous latch settings put RW at the same resistance setting prior to shutdown. This pin is logically AND with SHDN bit in ACR register. SPI interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.

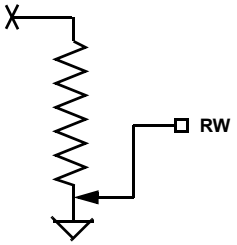


FIGURE 11. DCP CONNECTION IN SHUTDOWN MODE

Bus Interface Pins

SERIAL CLOCK (SCK)

This is the serial clock input of the SPI serial interface.

SERIAL DATA OUTPUT (SDO)

The SDO is an open drain serial data output pin. During a read cycle, the data bits are shifted out at the falling edge of the serial clock SCK, while the $\overline{\text{CS}}$ input is low.

SDO requires an external pull-up resistor for proper operation.

SERIAL DATA INPUT (SDI)

The SDI is the serial data input pin for the SPI interface. It receives device address, operation code, wiper address and data from the SPI external host device. The data bits are shifted in at the rising edge of the serial clock SCK, while the $\overline{\text{CS}}$ input is low.

CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ LOW enables the ISL22419, placing it in the active power mode. A HIGH to LOW transition on $\overline{\text{CS}}$ is required prior to the start of any operation after power up. When $\overline{\text{CS}}$ is HIGH, the ISL22419 is deselected and the SDO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.

Principles of Operation

The ISL22419 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and the SPI serial interface providing direct communication between host and potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR is recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer and internally connected to V_{CC} and GND. The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 7-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[6:0]: 00h), its wiper terminal (RW) is closest to GND. When the WR register of a DCP contains all ones (WR[6:0]: 7Fh), its wiper terminal (RW) is closest to V_{CC}. As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to GND to the closest to V_{CC}.

While the ISL22419 is being powered up, the WR is reset to 40h (64 decimal), which locates RW roughly at the center between GND and V_{CC}. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reload with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the SPI serial interface as described in the following sections.

Memory Description

The ISL22419 contains one non-volatile 7-bit register, known as the Initial Value Register (IVR), volatile 7-bit Wiper Register (WR), and volatile 8-bit Access Control Register (ACR). The memory map of ISL22419 is on Table 1. The non-volatile register (IVR) at address 0, contains initial wiper position and volatile register (WR) contains current wiper position.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	—	ACR
1	Reserved	
0	IVR	WR

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR[7]) determines whether the access is to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
BIT NAME	VOL	SHDN	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically AND with $\overline{SHDN}$ pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that non-volatile write operation is in progress. The WIP bit can be read repeatedly after a non-volatile write to determine if the write has been completed. It is impossible to write to the WR or ACR while WIP bit is 1.

Shutdown Mode

The device can be put in Shutdown mode either by pulling the $\overline{SHDN}$ pin to GND or setting the SHDN bit in the ACR register to 0. The truth table for Shutdown mode is in Table 3.

TABLE 3.

$\overline{SHDN}$ pin	SHDN bit	Mode
High	1	Normal operation
Low	1	Shutdown
High	0	Shutdown
Low	0	Shutdown

SPI Serial Interface

The ISL22419 supports an SPI serial protocol, mode 0. The device is accessed via the SDI input and SDO output with data clocked in on the rising edge of SCK, and clocked out on the falling edge of SCK. $\overline{CS}$ must be LOW during communication with the ISL22419. SCK and $\overline{CS}$ lines are controlled by the host or master. The ISL22419 operates only as a slave device.

All communication over the SPI interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

The first byte sent to the ISL22419 from the SPI host is the Identification Byte. A valid Identification Byte contains 0101 as the four MSBs, with the following four bits set to 0.

TABLE 4. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	0
(MSB)							(LSB)

The next byte sent to the ISL22419 contains the instruction and register pointer information. The four MSBs are the instruction and two LSBs are register address (see Table 5).

TABLE 5. IDENTIFICATION BYTE FORMAT

7	6	5	4	3	2	1	0
I3	I2	I1	I0	0	0	R1	R0

There are only two valid instruction sets:

1011(binary) - is a Read operation

1100(binary) - is a Write operation

There are only two registers address possible for this DCP. If the R1, R0 bits are zero, then the read or write is to either the IVR or the WR register (depends of VOL bit at ACR). If the R1 bit is 1and R0 bit is 0, then the operation is on the ACR.

Write Operation

A Write operation to the ISL22419 is a three-byte operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW, then a valid Identification Byte, then a valid instruction byte followed by Data Byte is sent to SDI pin. The host terminates the write operation by pulling the $\overline{CS}$ pin from LOW to HIGH. For a write to address 0 (WR), the byte at address 2 (ACR[7]) determines if the Data Byte is to be written to volatile or both volatile and non-volatile registers. Refer to “Memory Description” on page 9 and Figure 12.

The internal non-volatile write cycle starts after rising edge of $\overline{CS}$ and takes up to 20ms.

Read Operation

A read operation to the ISL22419 is a three byte operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW, then a valid Identification Byte, then a valid instruction byte followed by “dummy” Data Byte is sent to SDI pin. The SPI host reads the data from SDO pin on falling edge of SCK. The host terminates the read operation by pulling the $\overline{CS}$ pin from LOW to HIGH (see Figure 13).

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

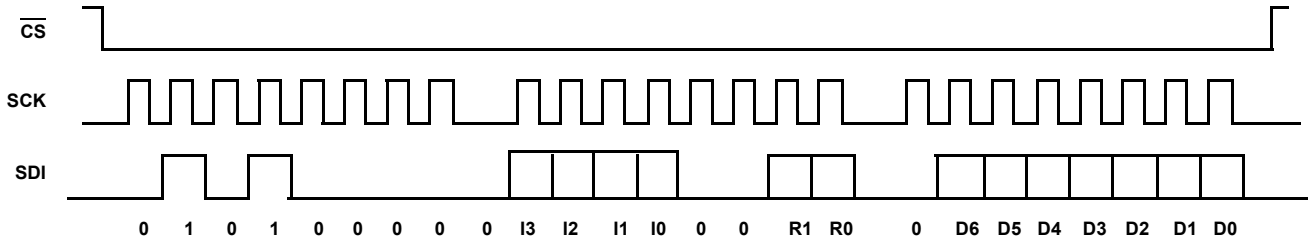


FIGURE 12. THREE BYTE WRITE SEQUENCE

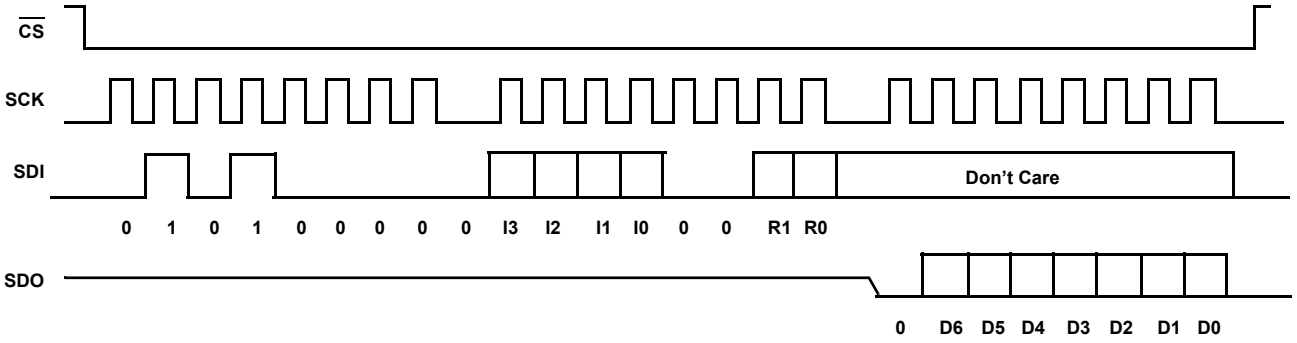


FIGURE 13. THREE BYTE READ SEQUENCE

Applications Information

Communicating with ISL22419

Communication with ISL22419 proceeds using SPI interface through the ACR (address 11b), IVR (address 00b) and WR (address 00b) registers.

The wiper of the potentiometer is controlled by the WR register. Writes and reads can be made directly to this register to control and monitor the wiper position without any non-volatile memory changes. This is done by setting MSB bit (ACR[7]) at address 11b to 1.

The non-volatile IVR stores the power up value of the wiper. IVR is accessible when MSB bit (ACR[7]) at address 11b is set to 0. Writing a new value to the IVR register will set a new power up position for the wiper. Also, writing to this register will load the same value into the WR as the IVR. Reading from the IVR will not change the WR, if its contents are different.

The typical application diagram is shown in Figure 14. For proper operation adding 0.1µF decoupling ceramic capacitor to V_{CC} is recommended. The capacitor value may vary based on expected noise frequency of the design.

Examples:

A. Writing to the IVR:

This sequence will write a new value (77h) to the IVR(non-volatile):

Set the ACR (Addr 02h) for NV write (40h)

Send the ID byte, Instruction Byte, then the Data byte

0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0

(Sent to SDI)

Set the IVR (Addr 00h) to 77h

Send the ID byte, Instruction Byte, then the Data byte

0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	1

(Sent to SDI)

B. Reading from the WR:

This sequence will read the value from the WR (volatile):

Write to ACR first to access the WR

Send the ID byte, Instruction Byte, then the Data byte

0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0

(Sent to SDI)

Read the data from WR (Addr 00h)

Send the ID byte, Instruction Byte, then Read the Data byte

0	1	0	1	0	0	0	0	1	0	1	1	0	0	0	0	x	x	x	x	x	x	x	x

(Out on SDO)

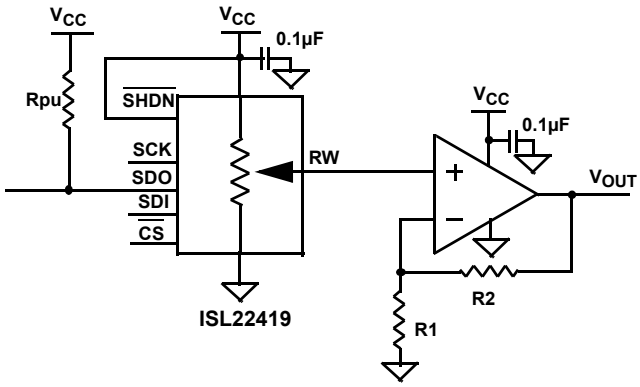
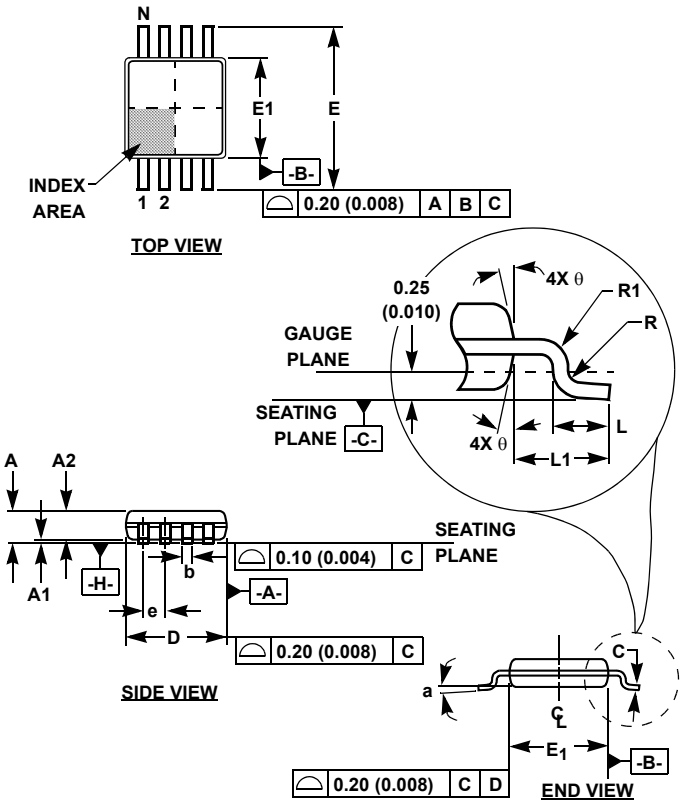


FIGURE 14. TYPICAL APPLICATION DIAGRAM FOR IMPLEMENTING ADJUSTABLE VOLTAGE REFERANCE

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A-] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.