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August 2015

# FDMS8095AC

## Dual N & P-Channel PowerTrench<sup>®</sup> MOSFET

N-Channel: 150 V, 27 A, 30 mΩ P-Channel: -150 V, -2.2 A, 1200 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 30 mΩ at  $V_{GS} = 10$  V,  $I_D = 6.2$  A
- Max  $r_{DS(on)}$  = 41 mΩ at  $V_{GS} = 6$  V,  $I_D = 5.2$  A

Q2: P-Channel

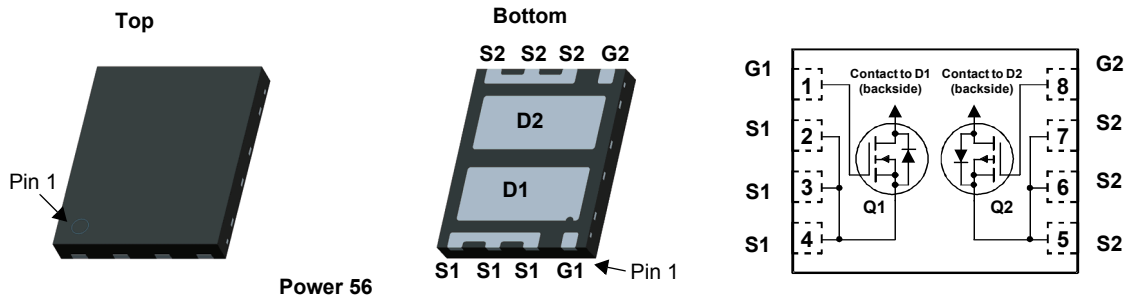
- Max  $r_{DS(on)}$  = 1200 mΩ at  $V_{GS} = -10$  V,  $I_D = -1$  A
- Max  $r_{DS(on)}$  = 1400 mΩ at  $V_{GS} = -6$  V,  $I_D = -0.9$  A
- Optimised for active clamp forward converters
- RoHS Compliant

### General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance. Shrinking the area needed for implementation of active clamp topology; enabling best in class power density.

### Applications

- DC-DC Converter
- Active Clamp



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units	
$V_{DS}$	Drain to Source Voltage	150	-150	V	
$V_{GS}$	Gate to Source Voltage	$\pm 20$	$\pm 25$	V	
$I_D$	Drain Current -Continuous	$T_C = 25^\circ\text{C}$ (Note 5)	27	-2.2	A
	Drain Current -Continuous	$T_C = 100^\circ\text{C}$ (Note 5)	17	-1.4	
	-Continuous	$T_A = 25^\circ\text{C}$	6.2 <sup>1a</sup>	-1 <sup>1b</sup>	
	-Pulsed	(Note 4)	143	-8.8	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	216	6	mJ
$P_D$	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$	2.3 <sup>1a</sup>	2.3 <sup>1b</sup>	W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$	0.9 <sup>1c</sup>	0.9 <sup>1d</sup>	
	Power Dissipation for Single Operation	$T_C = 25^\circ\text{C}$	50	12.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$	

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	55 <sup>1a</sup>	55 <sup>1b</sup>	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	138 <sup>1c</sup>	138 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	10	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8095AC	FDMS8095AC	Power 56	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$ $I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	150 -150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		103 122		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$ $V_{DS} = -120\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	Q1 Q2	2.0 -2.0	3.2 -3.2	4.0 -4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-11 -6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6.2\text{ A}$ $V_{GS} = 6\text{ V}$ , $I_D = 5.2\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 6.2\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q1		25 33 48	30 41 58	m $\Omega$
		$V_{GS} = -10\text{ V}$ , $I_D = -1\text{ A}$ $V_{GS} = -6\text{ V}$ , $I_D = -0.9\text{ A}$ $V_{GS} = -10\text{ V}$ , $I_D = -1\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q2		840 940 1520	1200 1400 2171	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{ V}$ , $I_D = 6.2\text{ A}$ $V_{DD} = -10\text{ V}$ , $I_D = -1\text{ A}$	Q1 Q2		19 0.75		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1		1441	2020	pF
			Q2		162	230	
$C_{oss}$	Output Capacitance	Q2	Q1		127	180	pF
			Q2		13	25	
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = -75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1		4.4	10	pF
			Q2		0.6	5	
$R_g$	Gate Resistance		Q1	0.1	1.3	3.3	$\Omega$
			Q2	0.1	3.3	8.3	

**Switching Characteristics**

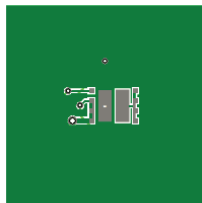
$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 75\text{ V}$ , $I_D = 6.2\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$	Q1		12	22	ns
			Q2		5.2	11	
$t_r$	Rise Time	Q2	Q1		2.7	10	ns
			Q2		1.6	10	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -75\text{ V}$ , $I_D = -1\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$	Q1		18	33	ns
			Q2		7.4	15	
$t_f$	Fall Time	Q2	Q1		4	10	ns
			Q2		6.3	13	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V}$ to $10\text{ V}$ $V_{GS} = 0\text{ V}$ to $-10\text{ V}$	Q1 Q2	$V_{DD} = 75\text{ V}$ , $I_D = 6.2\text{ A}$	21	30	nC
					2.8	4	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V}$ to $6\text{ V}$ $V_{GS} = 0\text{ V}$ to $-6\text{ V}$	Q1 Q2	$V_{DD} = 75\text{ V}$ , $I_D = 6.2\text{ A}$	13	19	nC
					1.8	2.6	
$Q_{gs}$	Gate to Source Charge	Q2 $V_{DD} = -75\text{ V}$ $I_D = -1\text{ A}$	Q1		6.7		nC
			Q2		0.8		
$Q_{gd}$	Gate to Drain "Miller" Charge	Q2 $V_{DD} = -75\text{ V}$ $I_D = -1\text{ A}$	Q1		3.9		nC
			Q2		0.7		

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

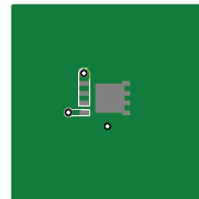
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 6.2\text{ A}$ (Note 2)	Q1		0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = -1\text{ A}$ (Note 2)	Q2		-0.9	-1.3	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 6.2\text{ A}, di/dt = 100\text{ A/s}$	Q1		69	111	ns
			Q2		44	71	
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = -1\text{ A}, di/dt = 100\text{ A/s}$	Q1		106	170	nC
			Q2		68	109	

### Notes:

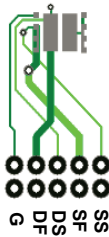
1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



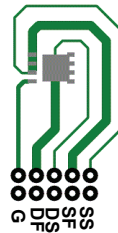
a.  $55\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $55\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



c.  $138\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper



d.  $138\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Q1:  $E_{AS}$  of 216 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 28\text{ A}$ .

Q2:  $E_{AS}$  of 6 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = -2\text{ A}$ ,  $V_{DD} = -150\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = -6.9\text{ A}$ .

4. Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

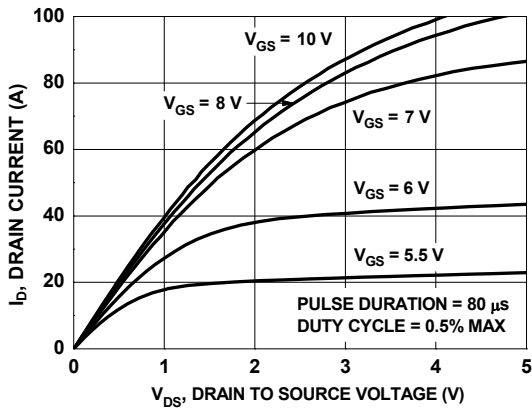


Figure 1. On Region Characteristics

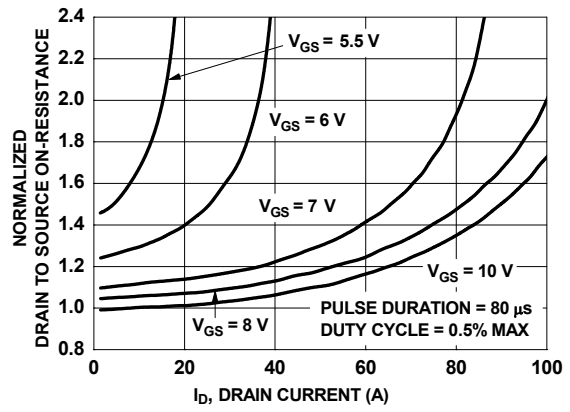


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

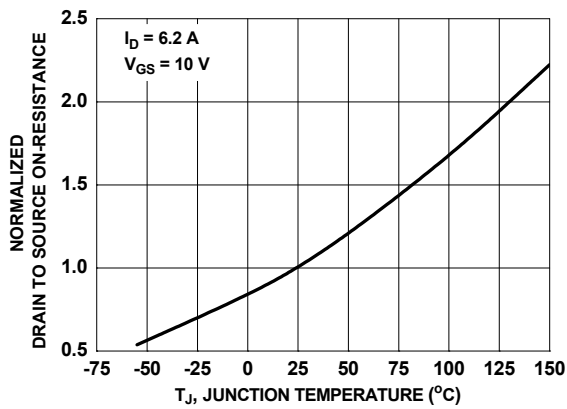


Figure 3. Normalized On Resistance vs Junction Temperature

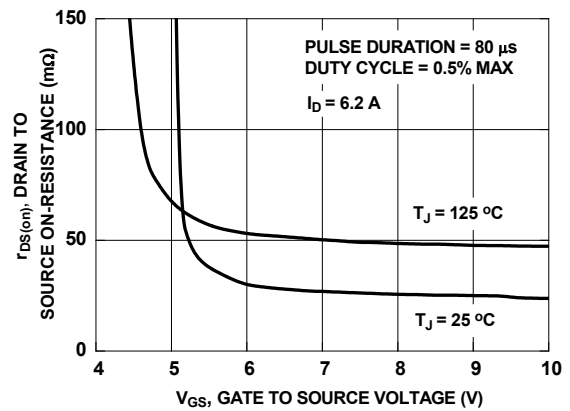


Figure 4. On-Resistance vs Gate to Source Voltage

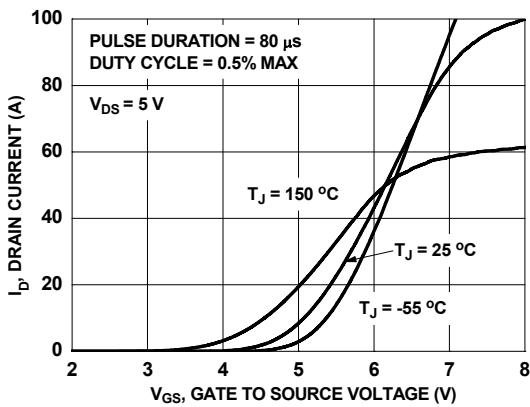


Figure 5. Transfer Characteristics

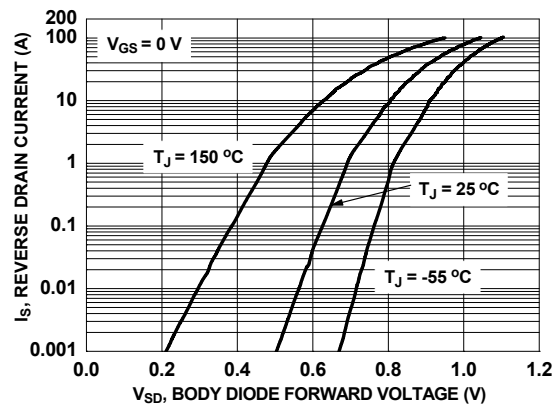
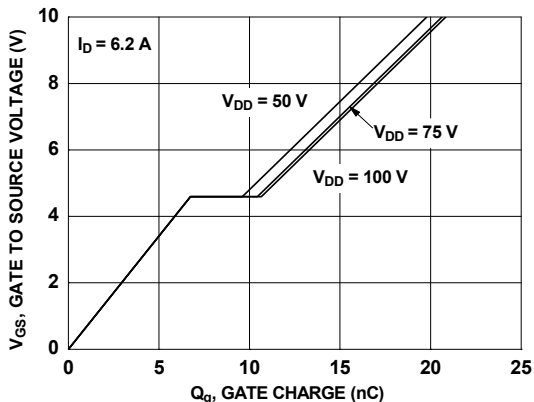
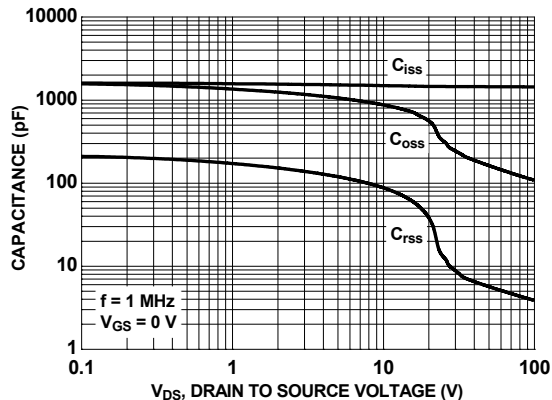


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

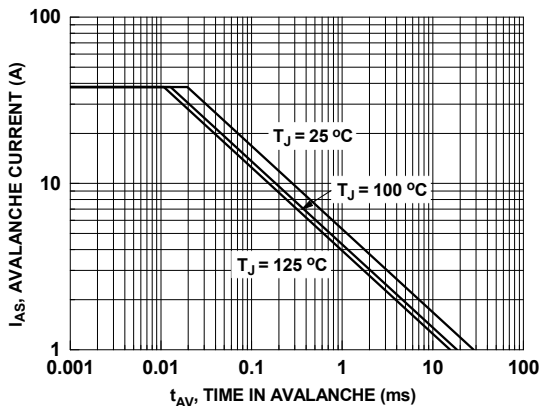
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



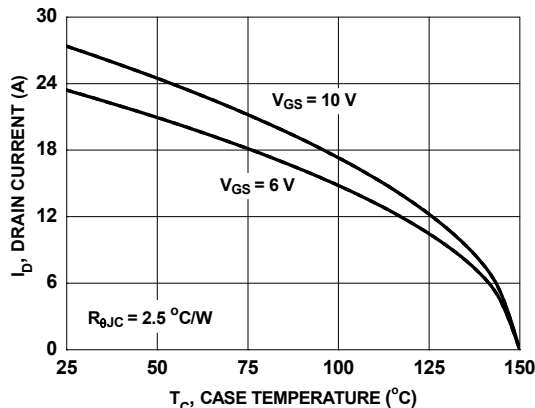
**Figure 7. Gate Charge Characteristics**



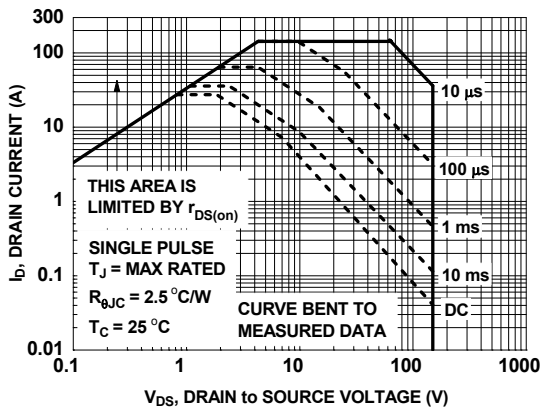
**Figure 8. Capacitance vs Drain to Source Voltage**



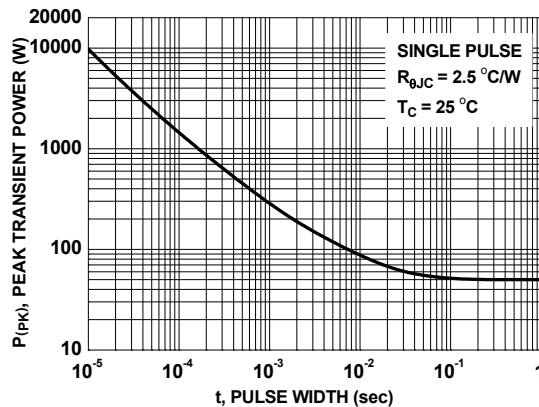
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

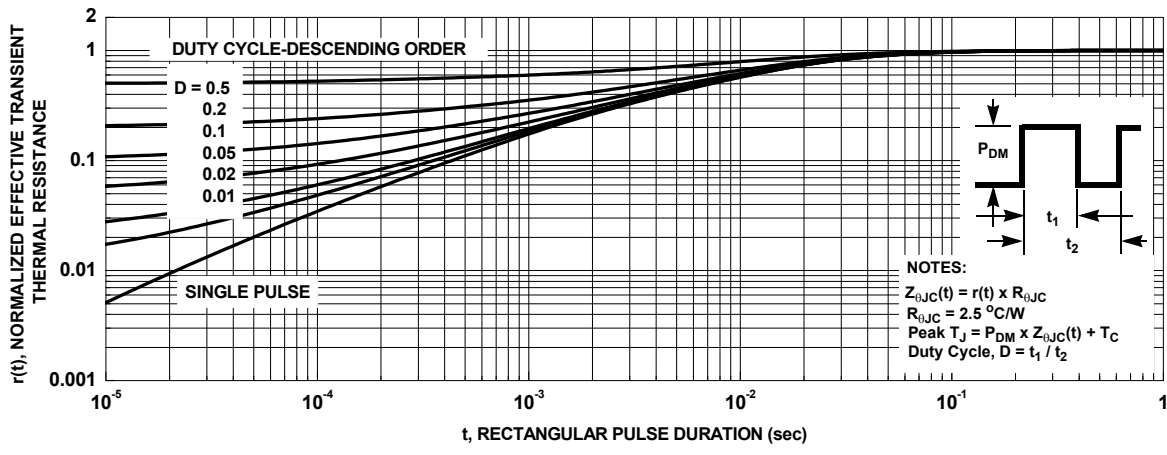


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

**Typical Characteristics (Q2 P-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

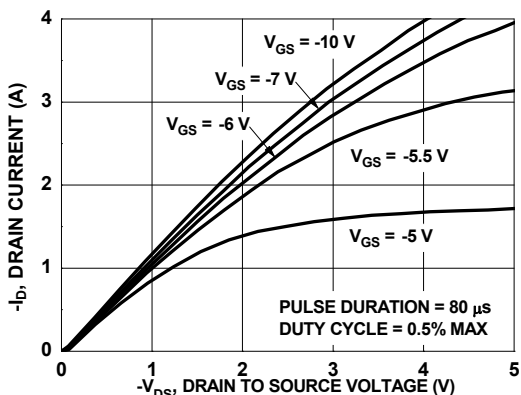


Figure 14. On-Region Characteristics

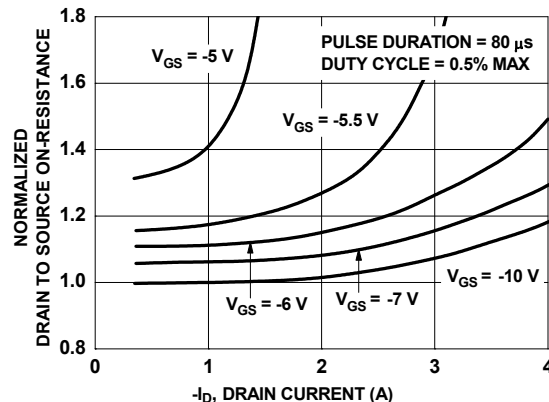


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

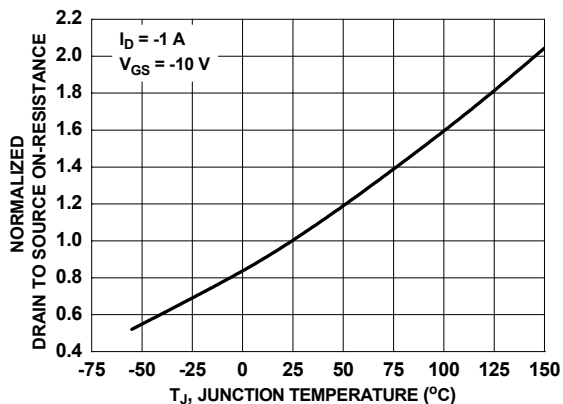


Figure 16. Normalized On-Resistance vs Junction Temperature

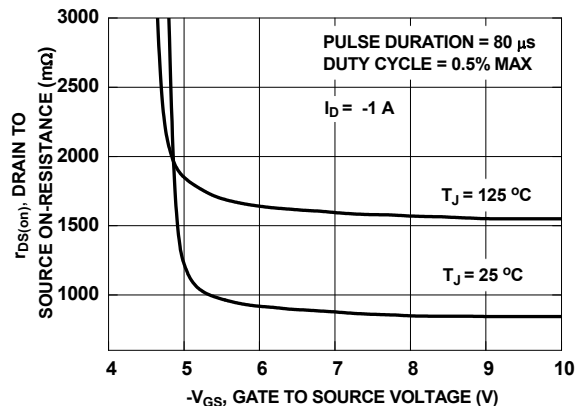


Figure 17. On-Resistance vs Gate to Source Voltage

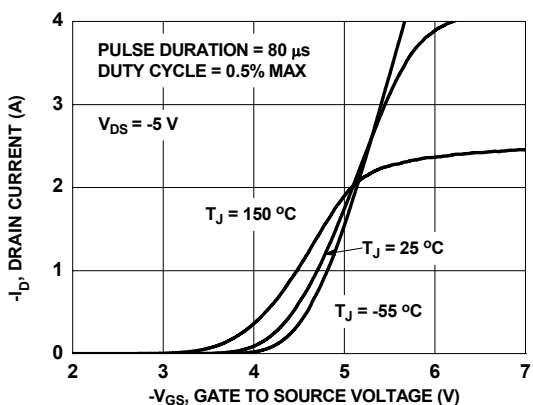


Figure 18. Transfer Characteristics

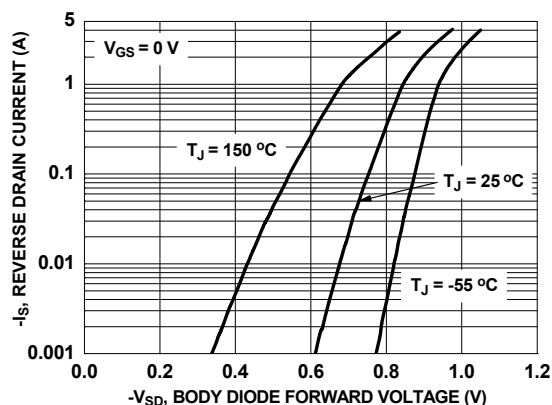
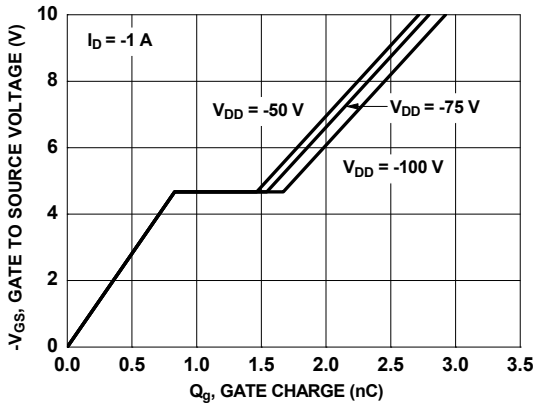


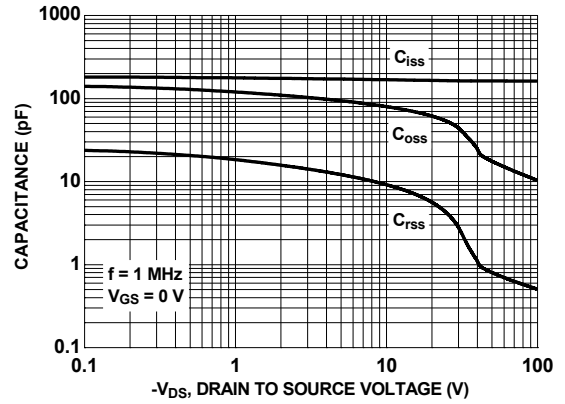
Figure 19. Source to Drain Diode Forward Voltage vs Source Current



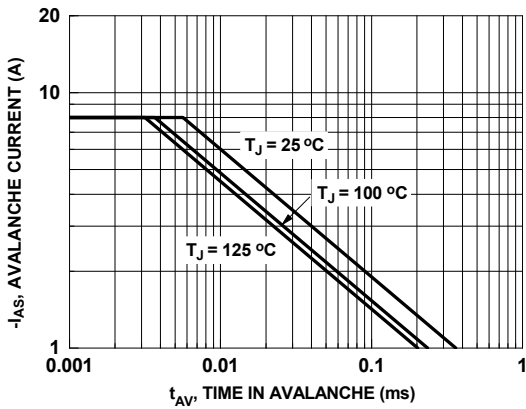
**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



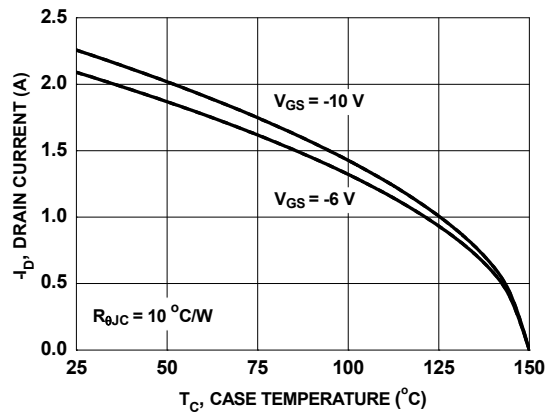
**Figure 20. Gate Charge Characteristics**



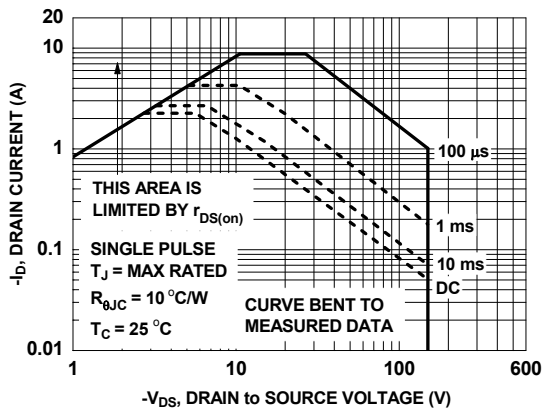
**Figure 21. Capacitance vs Drain to Source Voltage**



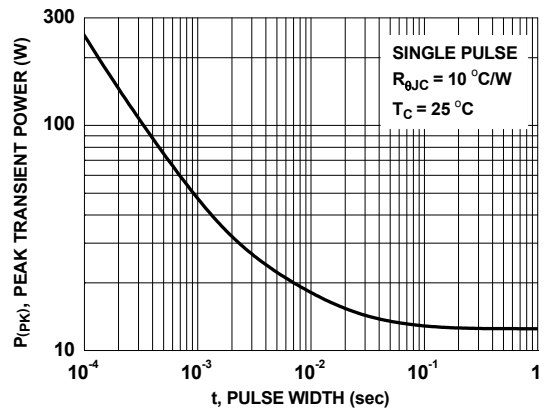
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs Case Temperature**

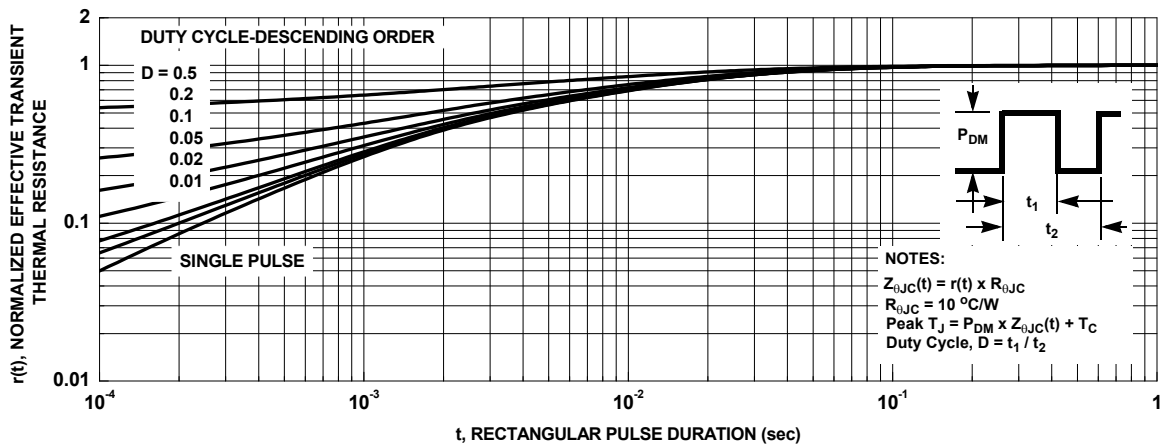


**Figure 24. Forward Bias Safe Operating Area**

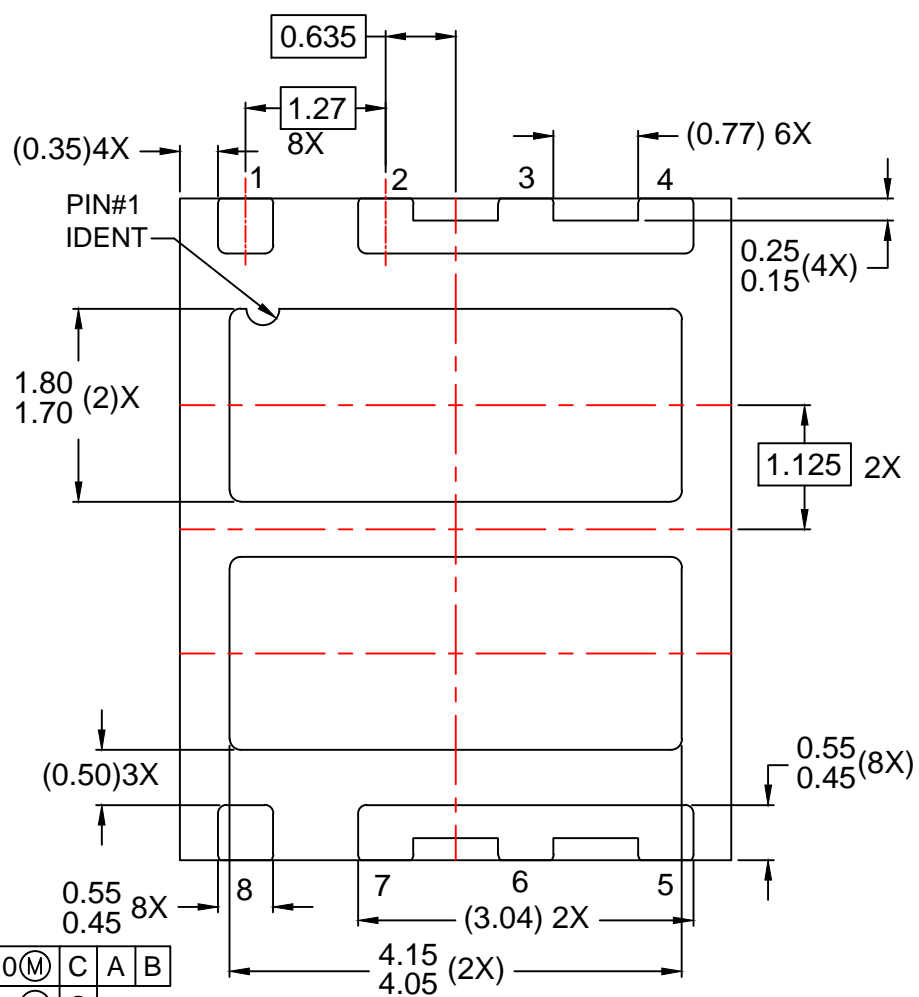
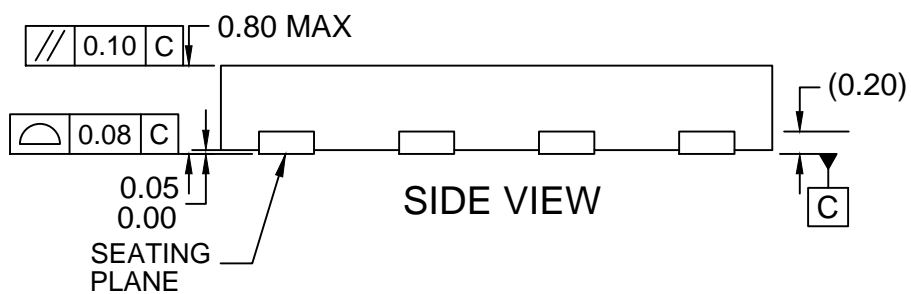
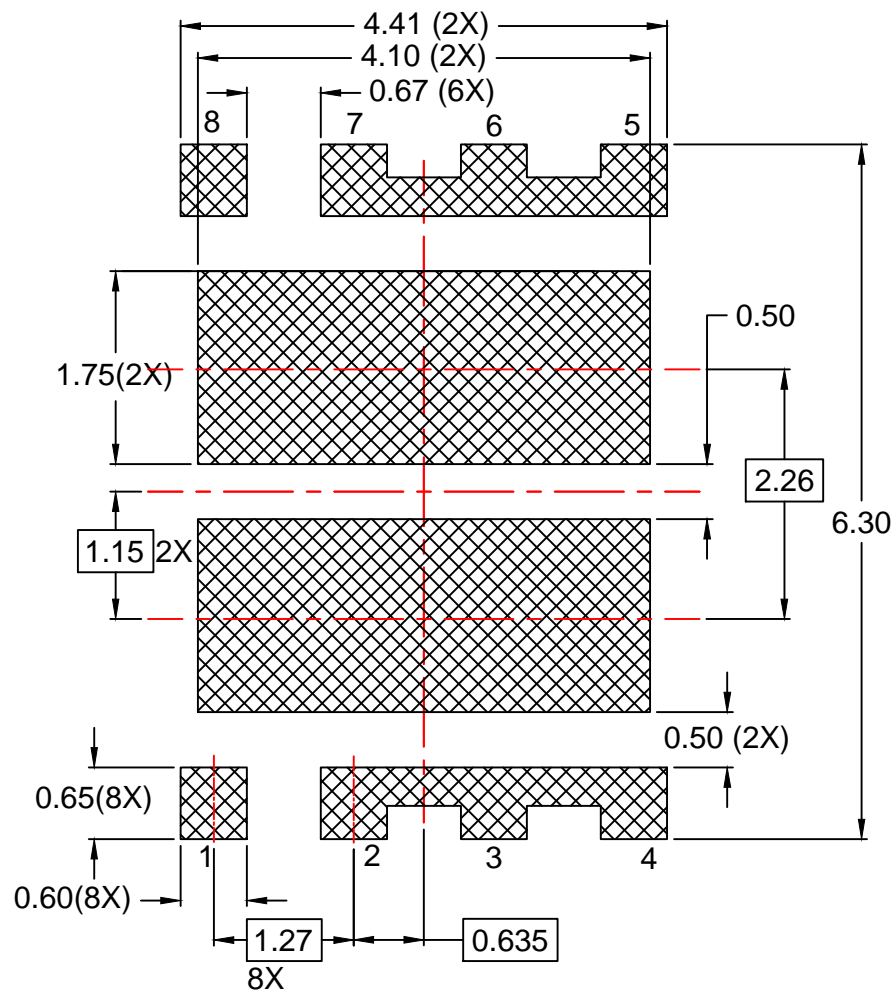
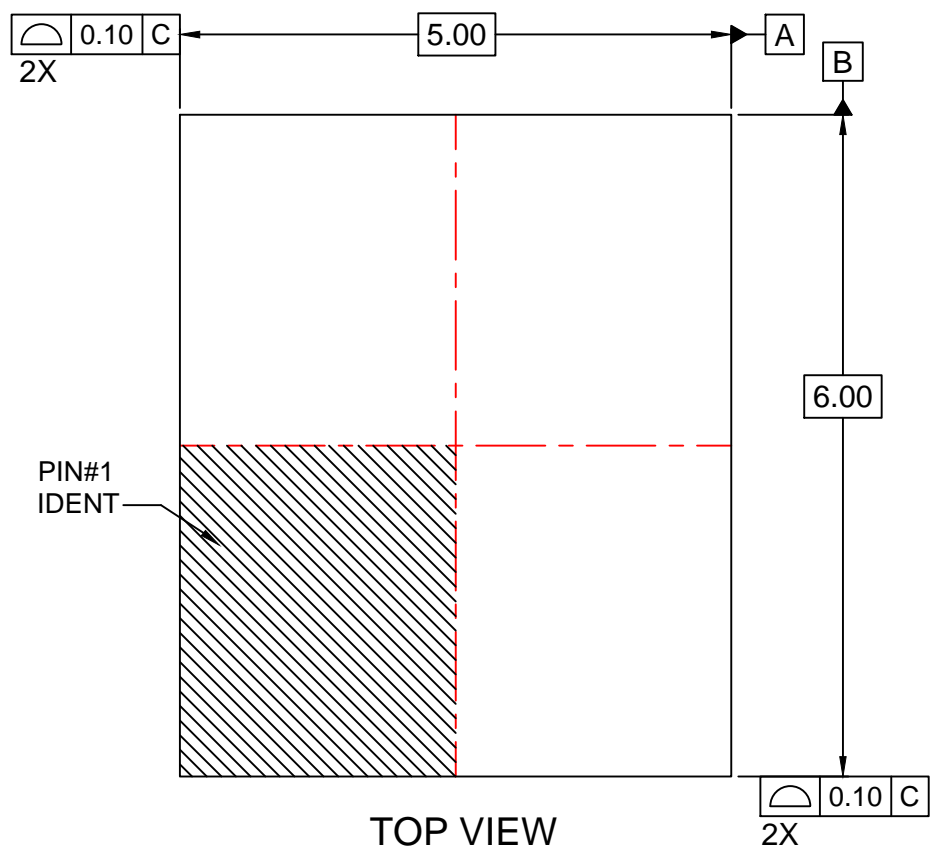


**Figure 25. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 P-Channel)  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted**



**Figure 26. Junction-to-Case Transient Thermal Response Curve**



⊕	0.10 (M)	C	A	B
	0.05 (M)	C		

- NOTES:**
- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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