MCF51JM128

32-bit ColdFire® USB microcontroller

Target Applications

- HVAC building and control systems
- Test and measurement equipment
- Environmental and building automation
- Security and access control panels
- Stationary barcode scanners and barcode printers
- PC peripherals and I/O modules
- Patient monitoring systems
- Laboratory equipment
- Industrial networking products
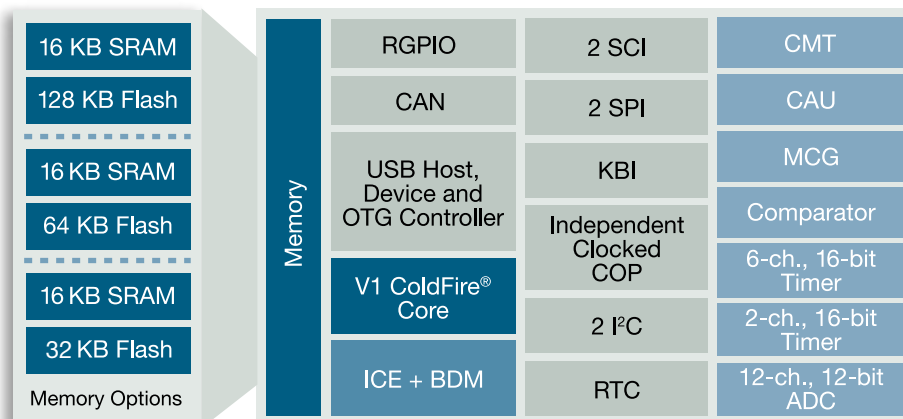- Hospital beds and electric wheel chairs

Overview

The MCF51JM128 is part of the Freescale Flexis™ microcontroller series, the connection point on the Freescale Controller Continuum where 8-bit and 32-bit compatibility becomes a reality. The Flexis series of devices includes complementary families of 8-bit S08 and 32-bit V1 ColdFire® microcontrollers that have a common set of peripherals and development tools to deliver migration flexibility.

The 32-bit MCF51JM128 device further extends the low-end of the ColdFire embedded USB controller family with up to 128 KB of flash memory, a full-speed USB 2.0 controller with host, device and On-The-Go (OTG) support, an integrated CAN module and a 12-channel, 12-bit analog-to-digital converter. The ColdFire JM family also features a hardware cryptographic acceleration unit (CAU), a random number generator accelerator (RNGA) and several system protection features such as low voltage detect and a Computer Operating Properly (COP) module.

The JM128 devices, like the other USB microcontrollers in the Controller Continuum, are supported by the Freescale USB-LITE Stack by CMX. This complimentary*** USB stack provides support for certain HID, CDC and mass storage classes. Source code for the complimentary stack is available. The MCF51JM128 is software compatible with other devices in the Controller Continuum, providing a direct migration path to higher performing USB microcontrollers.

MCF51JM128 Top-Level Block Diagram

Memory Options:
- 16 KB SRAM
- 128 KB Flash
- 16 KB SRAM
- 64 KB Flash
- 16 KB SRAM
- 32 KB Flash

Memory blocks: RGPIO, CAN, USB Host, Device and OTG Controller, V1 ColdFire® Core, ICE + BDM, 2 SCI, 2 SPI, KBI, Independent Clocked COP, 2 I²C, RTC, CMT, CAU, MCG, Comparator, 6-ch., 16-bit Timer, 2-ch., 16-bit Timer, 12-ch., 12-bit ADC

Features	Benefits
32-bit V1 ColdFire® Central Processing Unit (CPU)	
• Up to 50.33 MHz V1 ColdFire core offering 2.7 to 5.5V across a temperature range of -40°C to +105°C	• Offers strong performance throughout the entire voltage range
• ColdFire Instruction Set Revision C (ISA_C)	• Provides additional instructions for easy handling of 8-, 16- and 32-bit data
• Support for up to 30 peripheral interrupt requests and seven software interrupts	• Allows for software flexibility and optimization for real-time applications
On-Chip Memory	
• Up to 128K flash read/program/erase over full operating voltage and temperature	• Allows user to take full advantage of in-application, re-programmability benefits in virtually any environment
• Up to 16K RAM with security circuit	• Helps prevent unauthorized access to RAM • Flash contents helps to reduce system power consumption
Power-Saving Modes	
• Four low-power modes	• Allows continuation of sampling application in a reduced power state which helps to reduces system power consumption
• Multi-purpose clock generator (MCG)	• Frequency-locked loop (FLL): Internal or external reference can be used to control the FLL • Phase-locked loop (PLL): Voltage controlled oscillator (VCO). Modulo VCO frequency divider. Lock detector with interrupt capability. • Internal reference clock: Can be selected as the clock source for the MCU • External reference clock: Provides control for a separate crystal oscillator. Clock monitor with reset capability. Can be selected as the clock source for the MCU. • Reference divider provided • Clock source can be divided by 1, 2, 4 or 8
Peripherals	
• Dual-role USB On-The-Go (OTG) device, supports USB in either device, host or OTG configuration	• On-chip transceiver and 3.3V regualtor help save system cost, fully compliant with USB Specification 2.0. Allows control, bulk, interrupt and isochronous transfers
• Controller Area Network (CAN)	• Implementation of the CAN protocol—Version 2.0A/B. Five receive buffers with FIFO storage scheme. Three transmit buffers with internal prioritization using a "local priority" concept.
• Two serial communications interface (SCI) modules offering asynchronous communications	• Provides standard UART communications peripheral • Allows full-duplex, asynchronous, NRZ serial communication between MCU and remote devices

freescale™
semiconductor

Features / Benefits

Features	Benefits

Peripherals (continued)

- Cryptographic acceleration unit (CAU)
  - Supports DES, 3DES, AES, MD5 and SHA-1 cryptographic algorithms

- Random number generator accelerator (RNGA)
  - Generates 32-bit random numbers
  - Complies with FIPS-140 standards for randomness and non-determinism

- Analog comparators (ACMP)—One analog comparator with the option to compare to internal reference, output can be optionally routed to timer/pulse width modulation (TPM) as input capture trigger
  - Requires only single pin for input signal, freeing up other pin for other use
  - Allows other system components to see comparator result with minimal delay
  - Can be used for single slope ADC and RC time constant measurements

- Analog-to-digital converter (ADC)—12-channel, 12-bit resolution
  - Output formatted in 12-, 10- or 8-bit right-justified format
  - Single or continuous conversion
  - Operation in low power modes for lower noise operation
  - Asynchronous clock source for lower noise operation

- Two I²Cs with up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
  - Two I²C ports enable increased system memory by using an additional I²C EEPROM
  - Ability to add an additional I²C device

- SPI—Two serial peripheral interfaces with full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- SPI2 has 8 byte receive/transmit FIFO
  - Having two SPI allows two separate dedicated devices, for example, one SPI dedicated to a ZigBee® transceiver, and the other to MCUs or peripherals
  - Supports high-speed transmission minimizing CPU interrupts

- Carrier modulator timer (CMT)
  - Offers four modes of operation:
    - Time with independent control of high and low times
    - Baseband
    - Frequency shift key
    - Direct software control of IRO pin
  - Selectable input clock divide: 1, 2, 4 or 8

- TPM—Two timer modules with up to eight channels and 16-bit resolution
  - Each channel may be input capture, output compare or edge-aligned PWM
  - Input capture trigger on either rising or falling edge
  - Selectable polarity on PWM outputs
  - Timer clock source selectable as prescaled bus clock, fixed system clock or an external clock pin

Input/Output

- 16-bits of rapid general purpose input output (RGPIO)
  - Memory mapped I/O connected to core's local bus for fast toggle rates
  - Support for all access sizes

- Up to 8 keyboard interrupt (KBI) pins with selectable polarity
  - Each KBI pin is programmable as falling edge only, rising edge only, falling edge and low level or rising edge and high level interrupt sensitivity

- 66 GPIOs and one input-only and one output-only pin
  - Results in a large number of flexible I/O pins that allow vendors to easily interface the device into their own designs

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Allows the device to recognize run-away code (infinite loops) and resets the processor to help avoid lock-up states

- Low-voltage detection with reset or interrupt; selectable trip points
  - Alerts the developer to voltage drops outside of the typical operating range

- Illegal op code detection with reset
  - Allows the device to recognize erroneous code and resets the processor to help avoid lock-up states

- Flash block protection
  - Helps to prevent unauthorized access to flash RAM which greatly reduces the chance of losing vital system code for vendor applications

Hardware Development Support

- Classic ColdFire debug B+ functionality mapped into a single-pin BDM interface
  - Allows developers to use the same hardware cables between S08 and V1 ColdFire platforms

- Real-time debug support
  - Six hardware breakpoints which can be configured into a 1- or 2-level trigger with a programmable response (CPU halt or interrupt)

- Program trace support
  - Capture of processor status and debug data into on-chip trace buffer provides program trace capabilities and programmable start/stop recording conditions

Package Options

Part Number	Temp. Range	Package
MCF51JM128EVLK*	-40°C to +105°C	80-pin LQFP
MCF51JM128VLK	-40°C to +105°C	80-pin LQFP
MCF51JM128VQH	-40°C to +105°C	64-pin QFP
MCF51JM128VLH	-40°C to +105°C	64-pin LQFP
MCF51JM128VLD	-40°C to +105°C	44-pin LQFP
MCF51JM64EVLK*	-40°C to +105°C	80-pin LQFP
MCF51JM64VLK	-40°C to +105°C	80-pin LQFP
MCF51JM64VQH	-40°C to +105°C	64-pin QFP
MCF51JM64VLH	-40°C to +105°C	64-pin LQFP
MCF51JM64VLD	-40°C to +105°C	44-pin LQFP
MCF51JM32EVLK*	-40°C to + 105°C	80-pin LQFP
MCF51JM32VLK	-40°C to + 105°C	80-pin LQFP
MCF51JM32VQH	-40°C to + 105°C	64-pin QFP
MCF51JM32VLH	-40°C to + 105°C	64-pin LQFP
MCF51JM32VLD	-40°C to + 105°C	44-pin LQFP

Cost-Effective Development Tools DEMOJM
$99 USD**

Cost-effective demonstration kit featuring the ColdFire JM128 and the S08 JM60 daughter cards. Support for USB (host and device) and CAN. Built-in USB-BDM circuitry available for debugging and programming. USB-BDM circuitry includes serial communication and simple logic analyzer.

EVB51JM128
$325 USD**

Full-featured evaluation system for the ColdFire JM128 Flexis USB family. This evaluation system supports USB host, device and OTG as well as integrated CAN.

CodeWarrior™ Development Studio for Microcontrollers 6.1
Complimentary***

CodeWarrior Development Studio for Microcontrollers is an integrated tool suite that supports software development for Freescale's 8-bit or 32-bit microcontrollers. Designers can further accelerate application development with the help of the Processor Expert™ tool, which is an award-winning rapid application development tool in the CodeWarrior tool suite.

Freescale USB-LITE Stack by CMX
Complimentary***

Freescale is providing a comprehensive USB software solution through a complimentary USB stack. Freescale USB-LITE stack by CMX enables USB host and device modes of operation. The USB stack supports several HID and CDC to UART projects. The complimentary stack also interfaces with CodeWarrior Development Studio, providing a productive, comprehensive development environment for designing embedded applications.

* The device with CAU
** Prices indicated are MSRP
*** Subject to license agreement

Learn More: For more information about the Flexis JM family, please visit **www.freescale.com/flexis**.

freescale™
semiconductor