

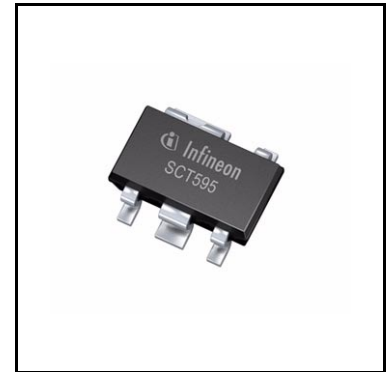
OPTIREG™ linear TLE4296-2

Low drop voltage regulator



Features

- Two output voltage versions: 3.3 V, 5.0 V
- Output voltage tolerance $\leq \pm 4\%$
- Very low drop voltage
- Output current: 30 mA
- Inhibit function
- Low quiescent current consumption
- Stable with ceramic output capacitor
- Input voltage up to 45 V
- Wide temperature range: $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$
- Output protected against short circuit
- Overtemperature protection
- Reverse polarity proof
- Very small and thermally enhanced package
- Green Product (RoHS compliant)



Potential applications

General automotive applications

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLE4296-2 is a monolithic integrated low drop voltage regulator in very small SMD package PG-SCT595-5. It is designed to supply various loads (e.g. microcontrollers, sensors, or as stand-by supply, etc.) under severe conditions. Therefore the device is equipped with additional protection functions against overload, short circuit and reverse polarity. In case of an overtemperature condition the regulator is automatically turned off by the integrated thermal protection circuit.

Input voltages up to 40 V are regulated to $V_{Q,nom} = 3.3$ V (V33 version) or 5.0 V (V50 version). The output is able to drive a load of 30 mA while it regulates the output voltage within a 4% accuracy. To save energy the device can be switched to stand-by mode via an inhibit input which causes the current consumption to drop below 5 μ A.

Type	Package	Marking
TLE4296-2GV33	PG-SCT595-5	C5
TLE4296-2GV50	PG-SCT595-5	C4

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Block diagram

1 Block diagram

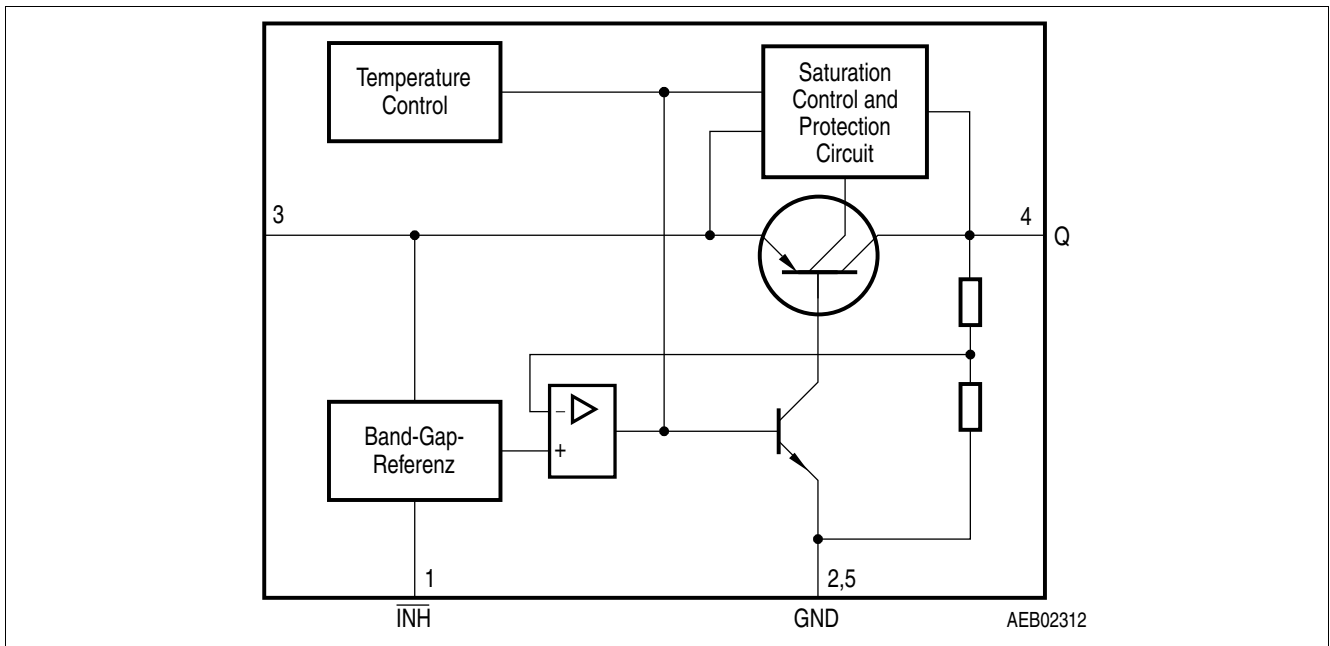


Figure 1 Block diagram

Pin configuration

2 Pin configuration

2.1 Pin assignment

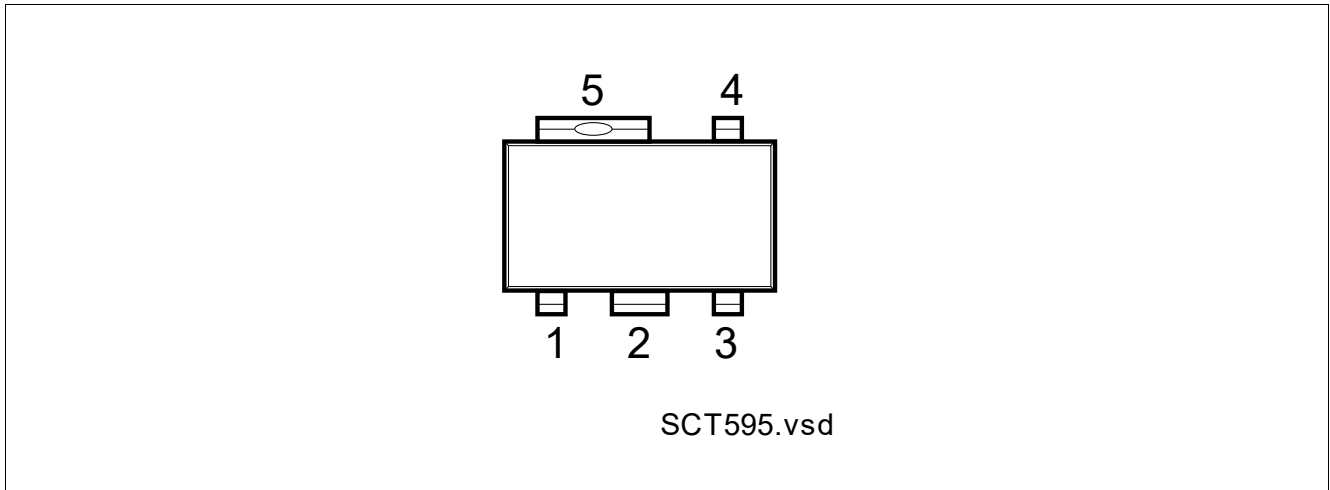


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	$\overline{\text{INH}}$	Inhibit input High level to turn on the IC.
2	GND	Ground Connected to pin 5.
3	I	Input voltage
4	Q	Output voltage Must be blocked with a ceramic capacitor $C_Q \geq 3.3 \mu\text{F}$, $\text{ESR} \leq 2 \Omega$.
5	GND	Ground Connected to pin 2.

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings¹⁾

$T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input							
Voltage	V_I	-42	–	45	V	–	P_3.1.1
Current	I_I	–	–	–		²⁾	
Output							
Voltage	V_Q	-0.3	–	30	V	–	P_3.1.2
Current	I_I	–	–	–		²⁾	
Inhibit							
Voltage	$V_{\overline{\text{INH}}}$	-42	–	45	V	–	P_3.1.3
Current	$I_{\overline{\text{INH}}}$	-500	–	²⁾	μA	–	P_3.1.4
		-5	–	5	mA	$-0.3\text{ V} \leq V_I \leq 45\text{ V};$ $t_p < 1\text{ ms}$	P_3.1.5
Temperatures							
Junction temperature	T_j	-40	–	150	$^\circ\text{C}$	–	P_3.1.6
Storage temperature	T_{stg}	-50	–	150	$^\circ\text{C}$	–	P_3.1.7
ESD susceptibility							
ESD resistivity to GND	V_{ESD}	-2	–	2	kV	HBM ³⁾	P_3.1.8

1) Not subject to production test, specified by design.

2) Internally limited.

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 k Ω , 100pF).

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

General product characteristics

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	4.0	–	45	V	TLE4296-2GV33	P_3.2.1
		5.5	–	45	V	TLE4296-2GV50	P_3.2.2
Inhibit voltage	V_{INH}	-0.3	–	40	V	–	P_3.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.4

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to ambient	R_{thJA}	–	179	–	K/W	Zero airflow zero heat sink area ¹⁾	P_3.4.1
Junction to soldering point	R_{thJSP}	–	30	–	K/W	measured to Pin 5	P_3.4.2

1) Worst case regarding peak temperature.

Electrical characteristics

4 Electrical characteristics

4.1 Electrical characteristics voltage regulator

Table 5 Electrical characteristics voltage regulator

$V_I = 13.5\text{ V}$; $V_{\text{INH}} > 2.5\text{ V}$; $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage TLE4296-2GV33	V_Q	3.17	3.30	3.43	V	$1\text{ mA} \leq I_Q \leq 30\text{ mA}$	P_5.1.1
		3.17	3.30	3.43	V	$I_Q = 10\text{ mA}$; $4.3\text{ V} \leq V_I \leq 40\text{ V}$	P_5.1.2
Output voltage TLE4296-2GV50	V_Q	4.80	5.00	5.20	V	$1\text{ mA} \leq I_Q \leq 30\text{ mA}$	P_5.1.18
		4.80	5.00	5.20	V	$I_Q = 10\text{ mA}$; $6\text{ V} \leq V_I \leq 40\text{ V}$	P_5.1.19
Output current limitation	I_Q	30	–	–	mA	¹⁾	P_5.1.3
Dropout voltage	V_{dr}	–	250	300	mV	$I_Q = 20\text{ mA}$	P_5.1.4
Output capacitor	C_Q	3.3	–	–	μF	$\text{ESR} \leq 2\ \Omega$ at 10 kHz	P_5.1.5
Current consumption $I_q = I_1 - I_Q$	I_q	–	2	5.2	mA	$I_Q < 30\text{ mA}$	P_5.1.6
		–	130	170	μA	$I_Q < 0.1\text{ mA}$; $T_j < 85^\circ\text{C}$	P_5.1.7
Quiescent current (stand-by) $I_q = I_1 - I_Q$	I_q	–	–	1	μA	$V_{\text{INH}} = 0.4\text{ V}$; $T_j < 85^\circ\text{C}$	P_5.1.8
		–	–	5	μA	$V_{\text{INH}} = 0.4\text{ V}$	P_5.1.9
Load regulation	ΔV_Q	–	17	50	mV	$1\text{ mA} < I_Q < 25\text{ mA}$; $T_j = 25^\circ\text{C}$; TLE4296-2GV50	P_5.1.21
		–	14	40	mV	$1\text{ mA} < I_Q < 25\text{ mA}$; $T_j = 25^\circ\text{C}$; TLE4296-2GV33	P_5.1.11
Line regulation	ΔV_Q	–	10	25	mV	$V_I = (V_{Q,\text{nom}} + 0.5\text{ V})$ to 36 V; $I_Q = 1\text{ mA}$; $T_j = 25^\circ\text{C}$	P_5.1.12
Power supply ripple rejection	PSRR	–	60	–	dB	$f_r = 100\text{ Hz}$; $V_r = 0.5\text{ V}_{\text{pp}}$	P_5.1.13

Logic Inhibit input

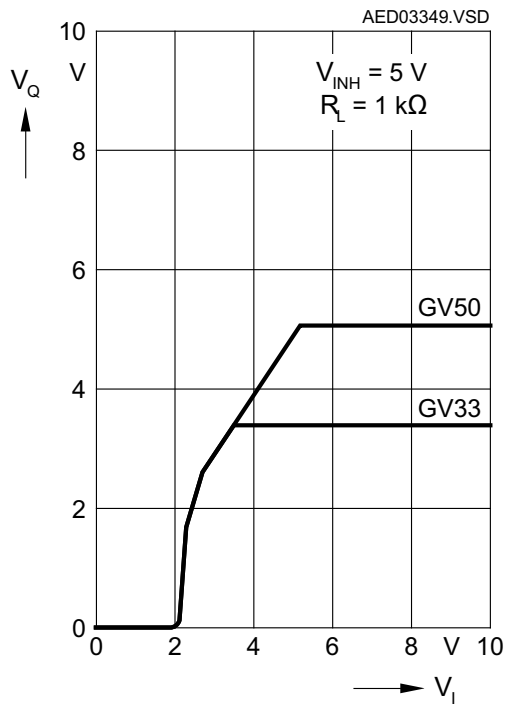
Inhibit, turn-on voltage	$V_{\text{INH,high}}$	–	–	2.2	V	$V_Q > 0.95 \times V_{Q,\text{nom}}$	P_5.1.14
Inhibit, turn-off voltage	$V_{\text{INH,low}}$	0.4	–	–	V	$V_Q < 0.1\text{ V}$	P_5.1.15
H-input current	$V_{\text{INH,high}}$	–	8	12	μA	$V_{\text{INH}} = 5\text{ V}$	P_5.1.16
L-input current	$V_{\text{INH,low}}$	-2	–	2	μA	$V_{\text{INH}} = 0\text{ V}$	P_5.1.17

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value.

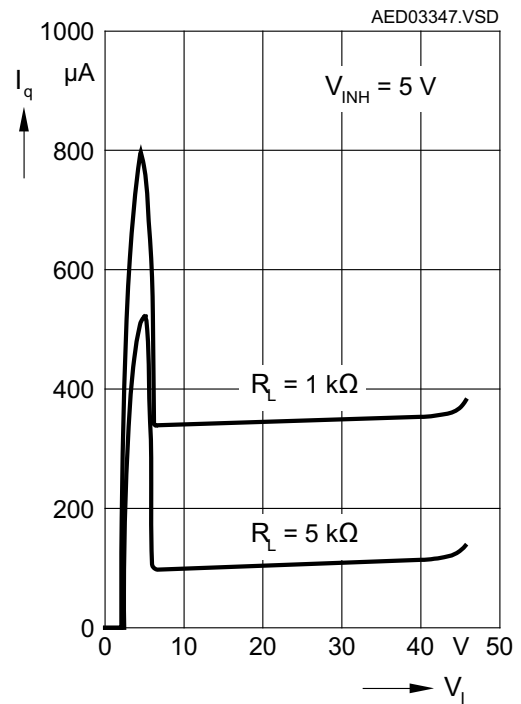
Electrical characteristics

4.2 Typical performance characteristics voltage regulator

Output voltage V_Q vs. input voltage V_I



Current consumption I_q vs. input voltage V_I



Application information

5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

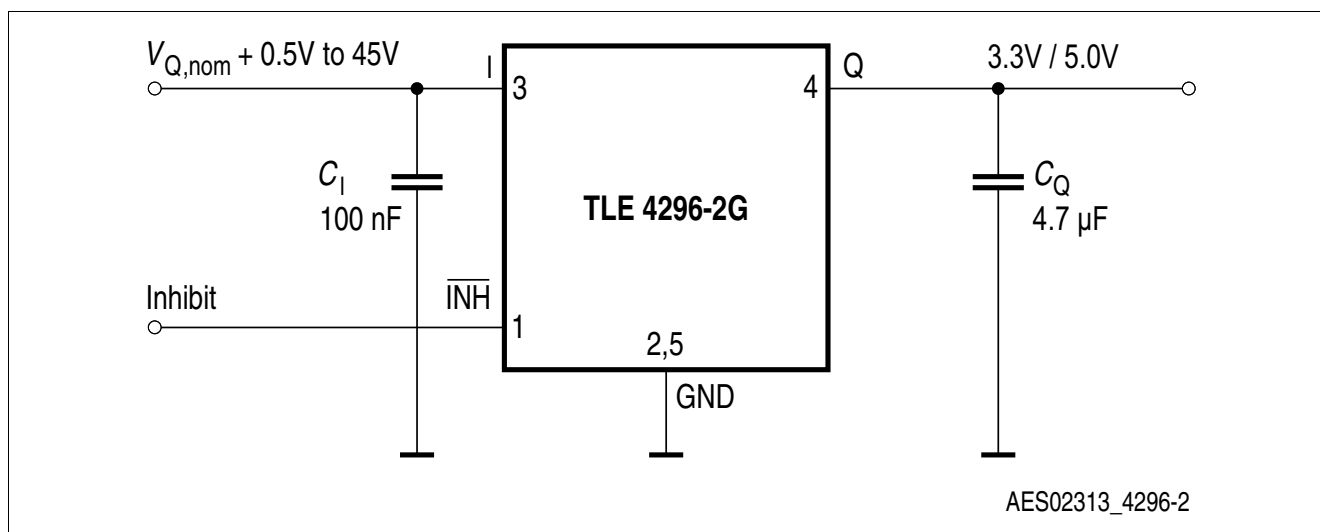


Figure 3 Application diagram

The output voltage of the TLE4296-2 is divided and compared to an internal reference of 2.5 V typical. A regulation loop controls the output to achieve a stabilized output voltage.

Figure 3 shows a typical application circuit. In order to maintain the stability of the control loop the TLE4296-2 output requires an output capacitor C_Q of at least 3.3 μF with a maximum permissible ESR of 2 Ω . It is recommended to use a multi layer ceramic capacitor for C_Q , e.g. the TDK C3216X7R1C475M with a nominal capacitance of 4.7 μF . Aluminum electrolytic as well as tantalum capacitors do not cover the required ESR range over the full operating temperature range of $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$.

At the input of the regulator a capacitor is required for compensating line influences (100 nF ceramic capacitor recommended). A resistor of approximately 1 Ω in series with the input capacitor C_I can dampen oscillations that could occur due to the input line inductance and the input capacitor. If the regulator is sourced via long input lines of several meters it is recommended to place an additional electrolytic capacitor $\geq 47 \mu\text{F}$ at the input.

6 Package information

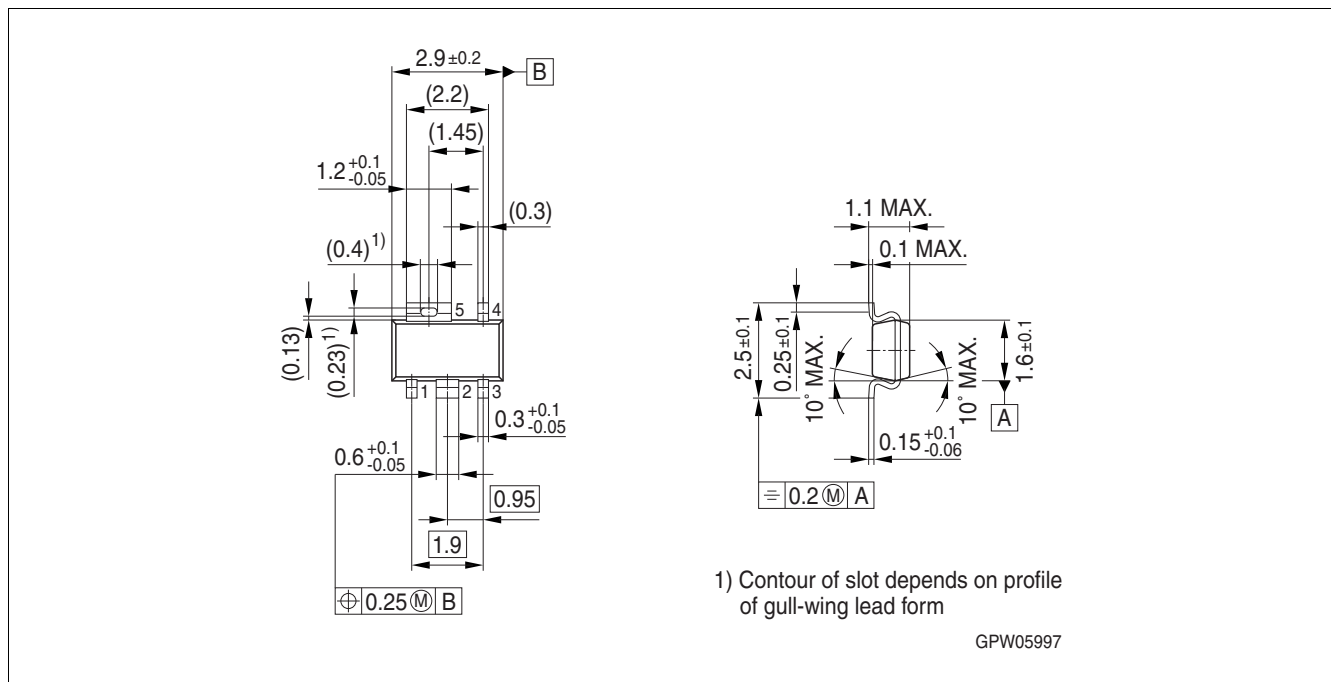


Figure 4 PG-SCT595-5¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

Revision history

7 Revision history

Revision	Date	Changes
1.21	2023-05-10	Editorial change
1.20	2021-05-11	Updated layout and structure Editorial changes Corrected typo at PSSR parameter Added TOC
1.13	2014-03-18	Typo (introduced in Rev. 1.11) in unit of parameter P_4.1.6 corrected from A to mA. No change of the device or test limits
1.12	2011-05-11	FrontCover: Current consumption in stand-by corrected from 5 mA to 5 mA in the functional description. Value in electrical characteristics is still correct
1.11	2011-02-10	FrontCover: Marking added Coverpage added All pages: New Infineon datasheet layout applied
1.1	2008-01-28	Initial version of RoHS-compliant derivate of TLE 4296-2(FrontCover): AEC certified statement added. FrontCover and Package outlines: RoHS compliance statement and Green product feature added. Package changed to RoHS compliant version Legal disclaimer updated
1.0	2004-01-01	Final datasheet

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Edition 2023-05-10

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

Z8F50302867

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